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EDN®

Designer's guide to flash-ADC testing—Pt 2

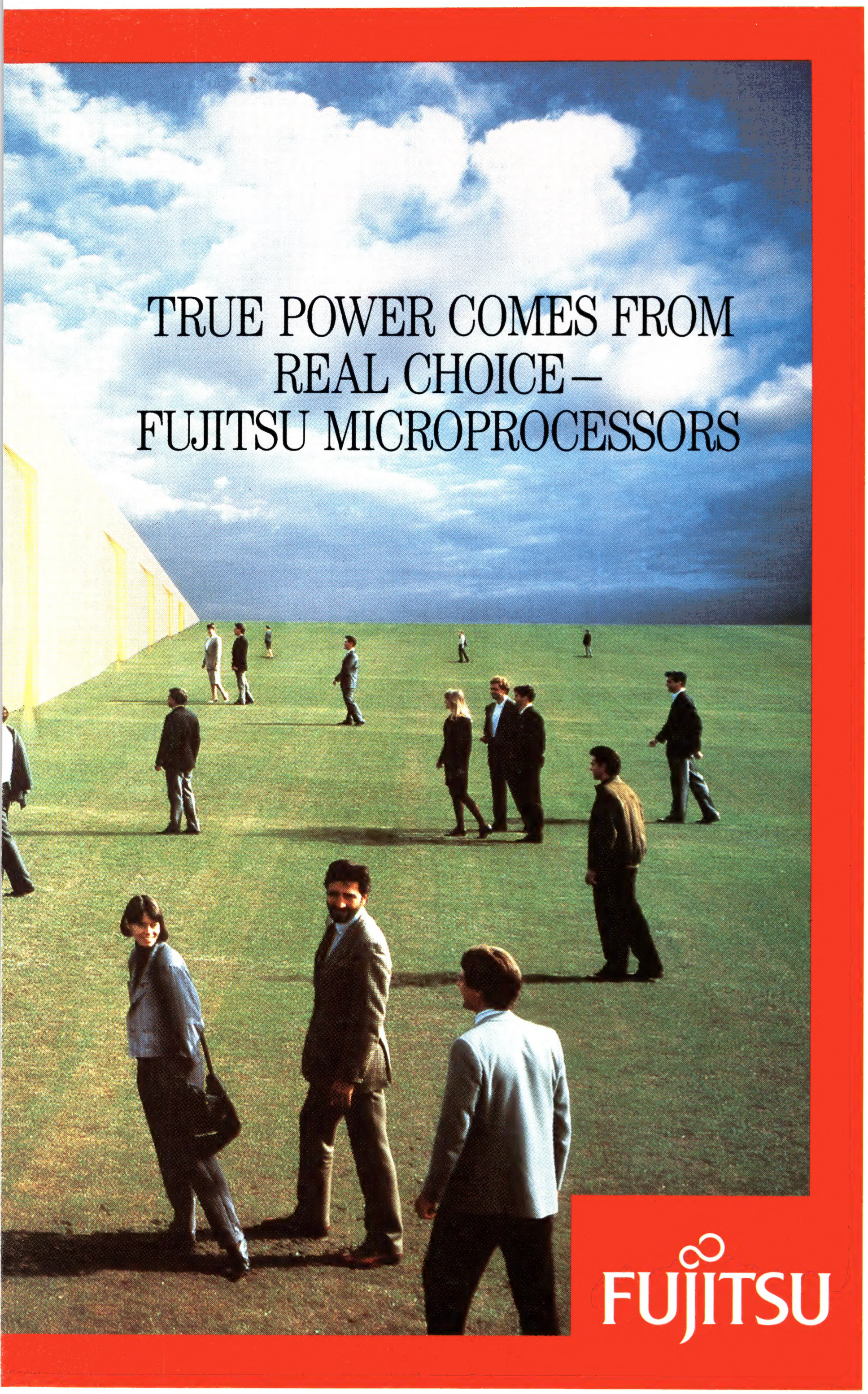
Engineering in Germany

New CASE packages for embedded systems

Designing step-down switching regulators

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Voltage references withstand the test of time and temperature



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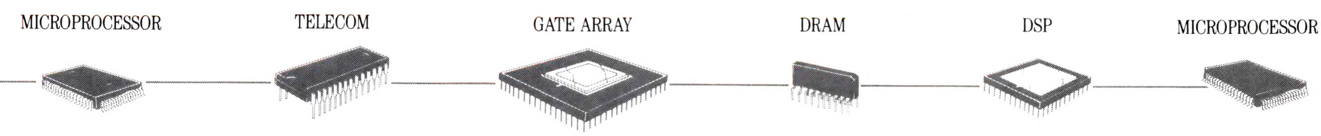

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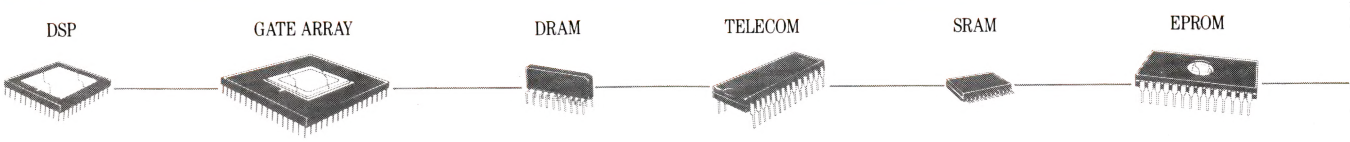
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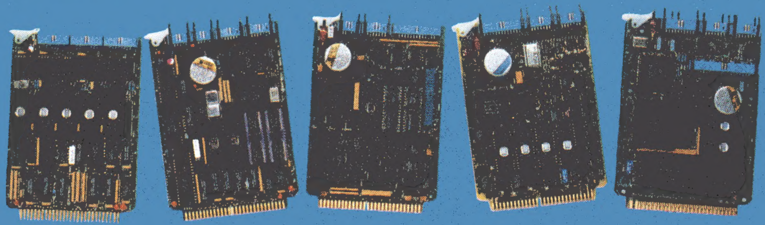

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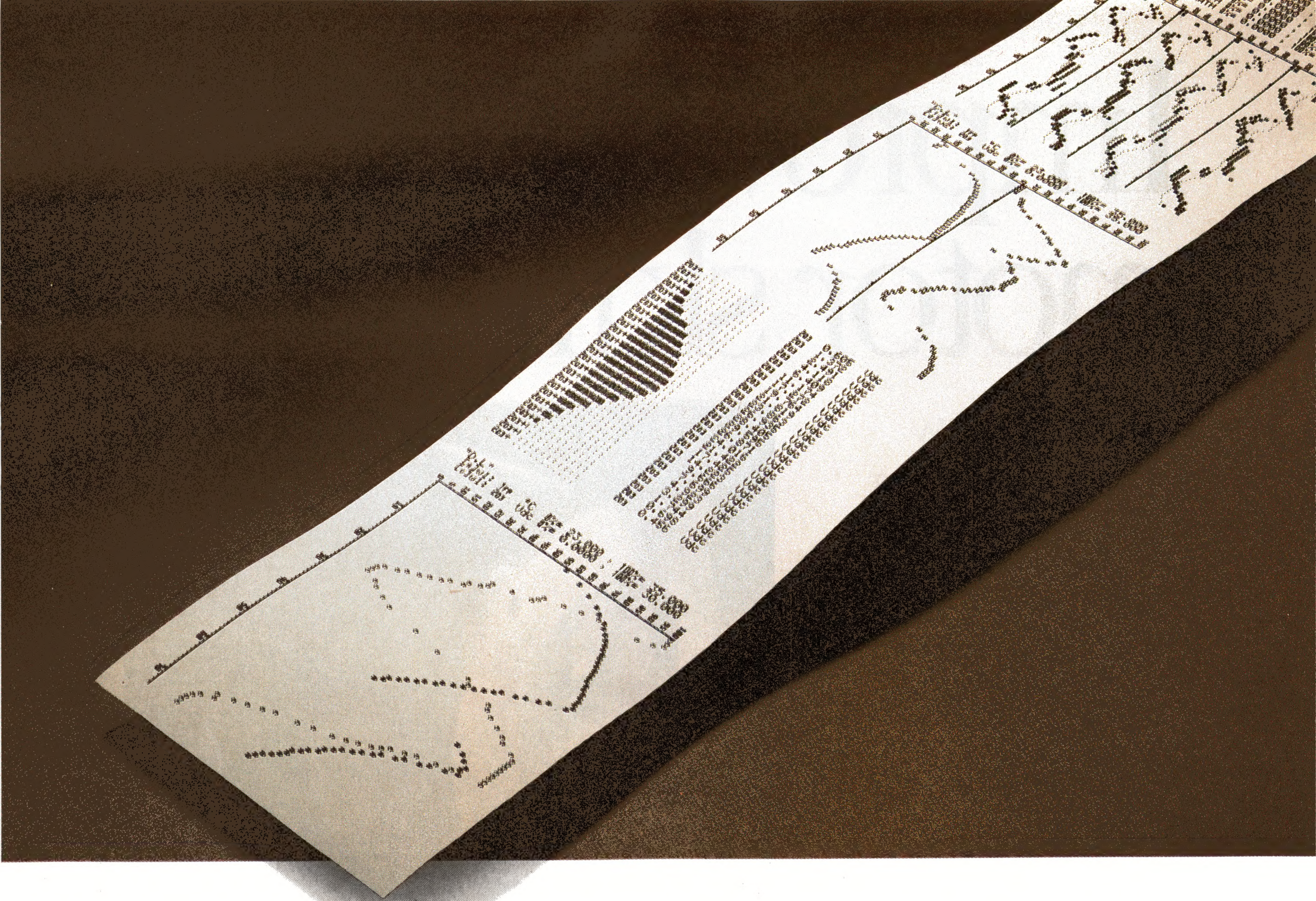

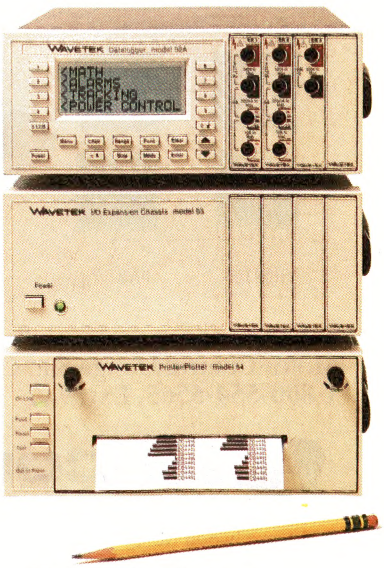
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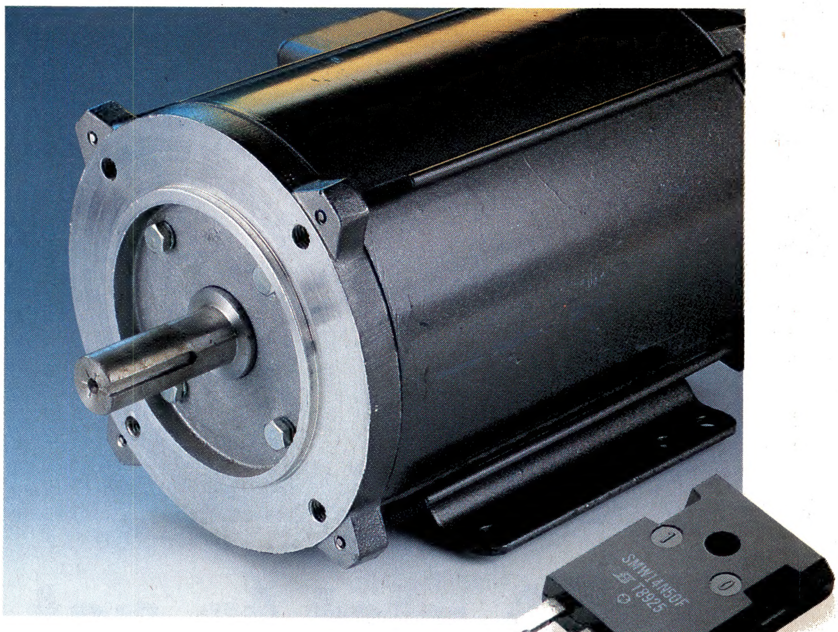

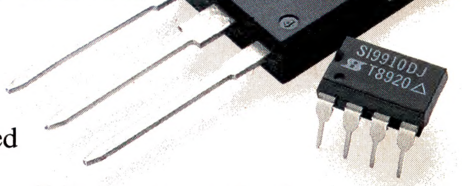

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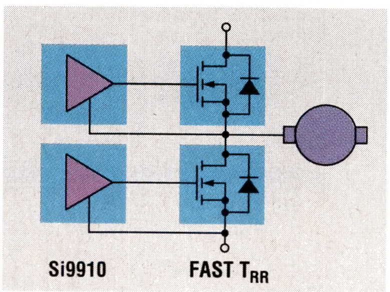

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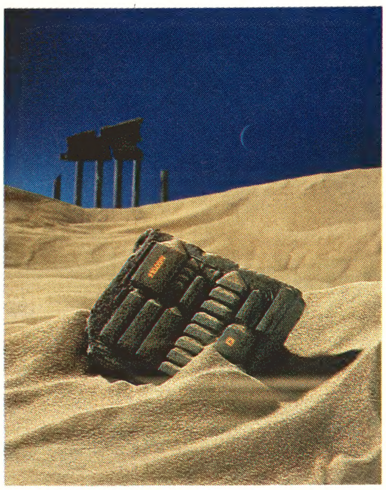
EDN® Magazine Edition

Volume 35, Number 2

Janurary 18, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Manufacturers offer a wide range of voltage references to suit various environments. Keep in mind the characteristics that are important to your particular application when you make your choice. See the Special Report on pg 120. (Photo courtesy Analog Devices Inc)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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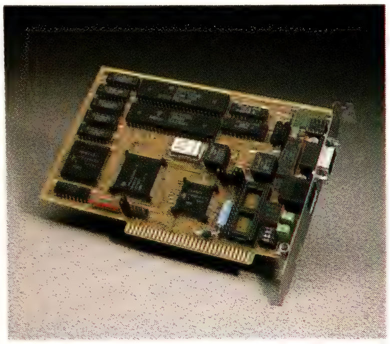
Circle 48 for Employment Information



***You can expect to see more token-ring LANs** in non-IBM installations—the availability of faster boards is one reason why (pg 65).*

TECHNOLOGY UPDATES

Expect token-ring LANs to become more popular beyond IBM installations because of the benefits they offer compared with Ethernet networks. Speed, reliability, and improved bandwidth performance are a few reasons token-ring boards are expanding their realm of applications.—*Maury Wright, Regional Editor*

Finally there's a worthwhile alternative to the time-consuming and tedious task of keying data and text into your personal computer by hand. Recently introduced, inexpensive software—optical-character-recognition packages—can accurately transform the printed output of high-resolution optical scanners into an ASCII file in your computer. —*Charles H Small, Senior Editor*

To avoid extensive redesign tasks, you must maintain a delicate balance between software and hardware development when designing for embedded systems. Four new computer-aided-software-engineering (CASE) packages, however, may simplify and speed the process. And unlike structured-analysis packages for batch-processing systems, these new tools concentrate specifically on code writing, debug, integration, and performance evaluation.—*Margery Conner, Regional Editor*

PRODUCT UPDATES

DESIGN IDEAS

Continued on page 9

Cahners Publishing Company, A Division of Reed Publishing USA ☐ Specialized Business Magazines for Building & Construction ☐ Manufacturing ☐ Foodservice & Lodging ☐ Electronics & Computers ☐ Interior Design ☐ Printing ☐ Publishing ☐ Industrial Research & Technology ☐ Health Care ☐ and Entertainment. Specialized Consumer Magazines: ☐ American Baby ☐ and Modern Bride.

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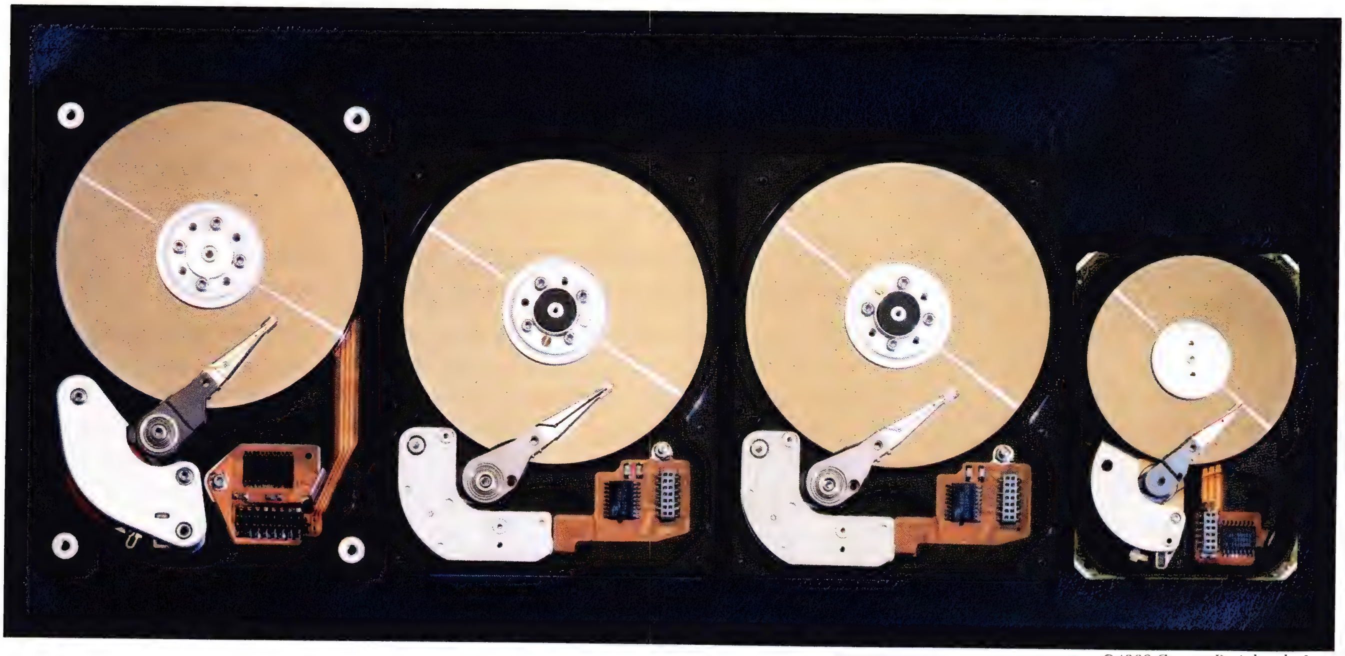

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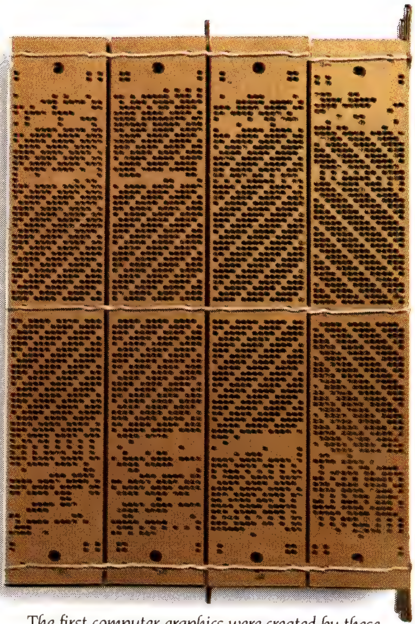
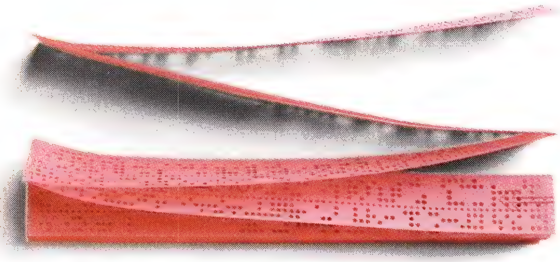
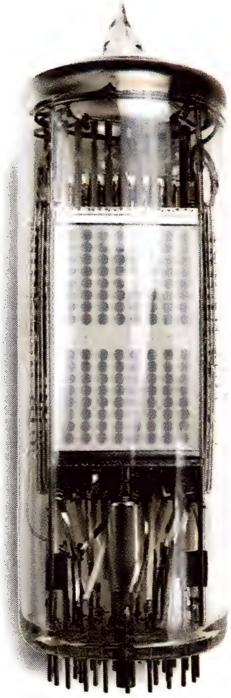


The first computer graphics were created by these cards designed for use on the Jacquard loom in the late 18th Century.

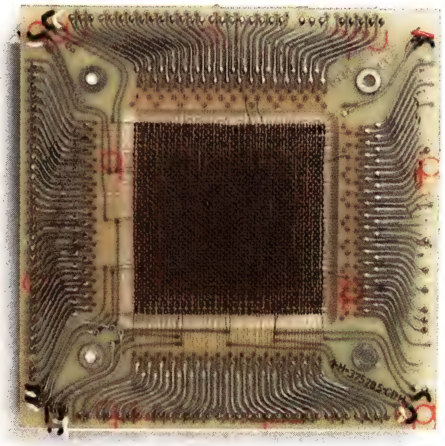


Each 2.5 x 21.5 cm section has a whopping 1360 possible digits. Users of paper tape were probably the first to pray for a paperless office.



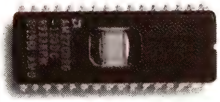
The Selectron tube had random access to 256 bits of storage with a cycle time of a mere 20ms.

Keep up with with AMD's fast



IBM® used 64 of these core memory planes in the 1958 SAGE.

This disk is one of six from a 1956 IBM 1316 disk pack which stored 2 million bits and accessed data at an astonishing 250ms.



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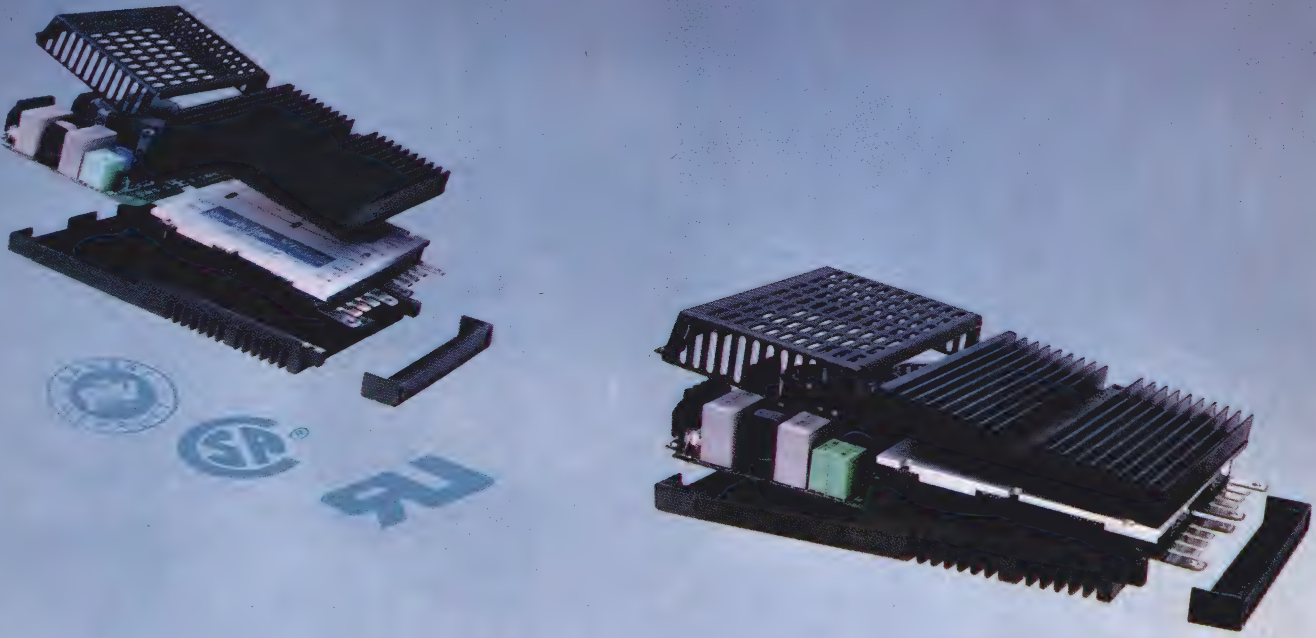

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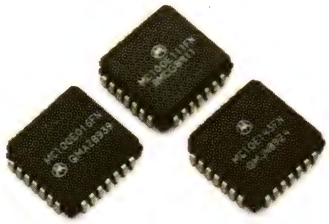
E112	Quad Driver	700ps
E116	5-bit Diff. Line Rcvr.	500ps
E131	4-bit Flip-flop	800 MHz
E141	8-bit Shift Register	700 MHz
E241	8-bit Scannable Register	700 MHz
E151	6-bit D Register	800 MHz
E156	3-bit 4:1 Mux-Latch	950 ps
E163	2-bit 8:1 Mux	850 ps
E451	6-bit Diff. Register	800 MHz

*within-device skew



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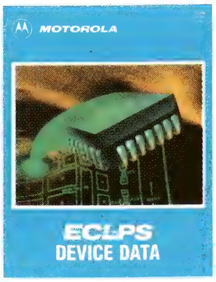

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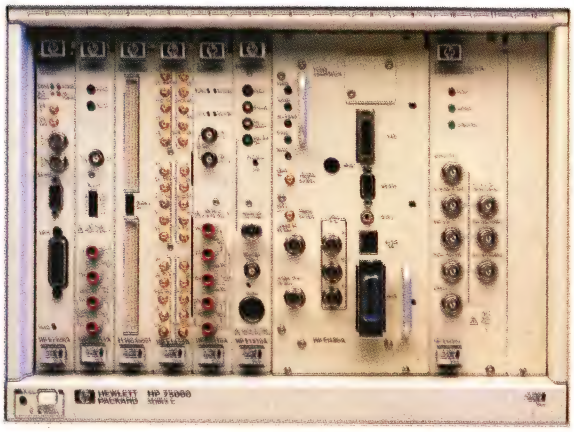

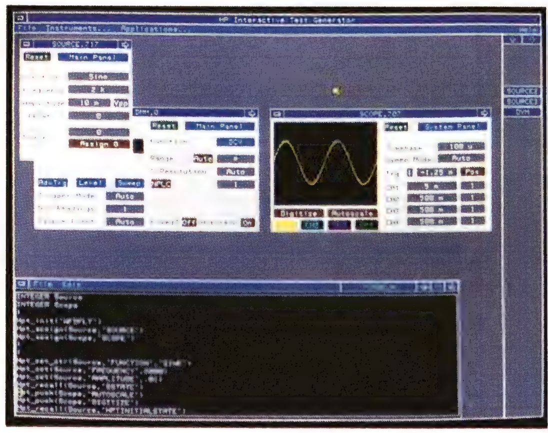

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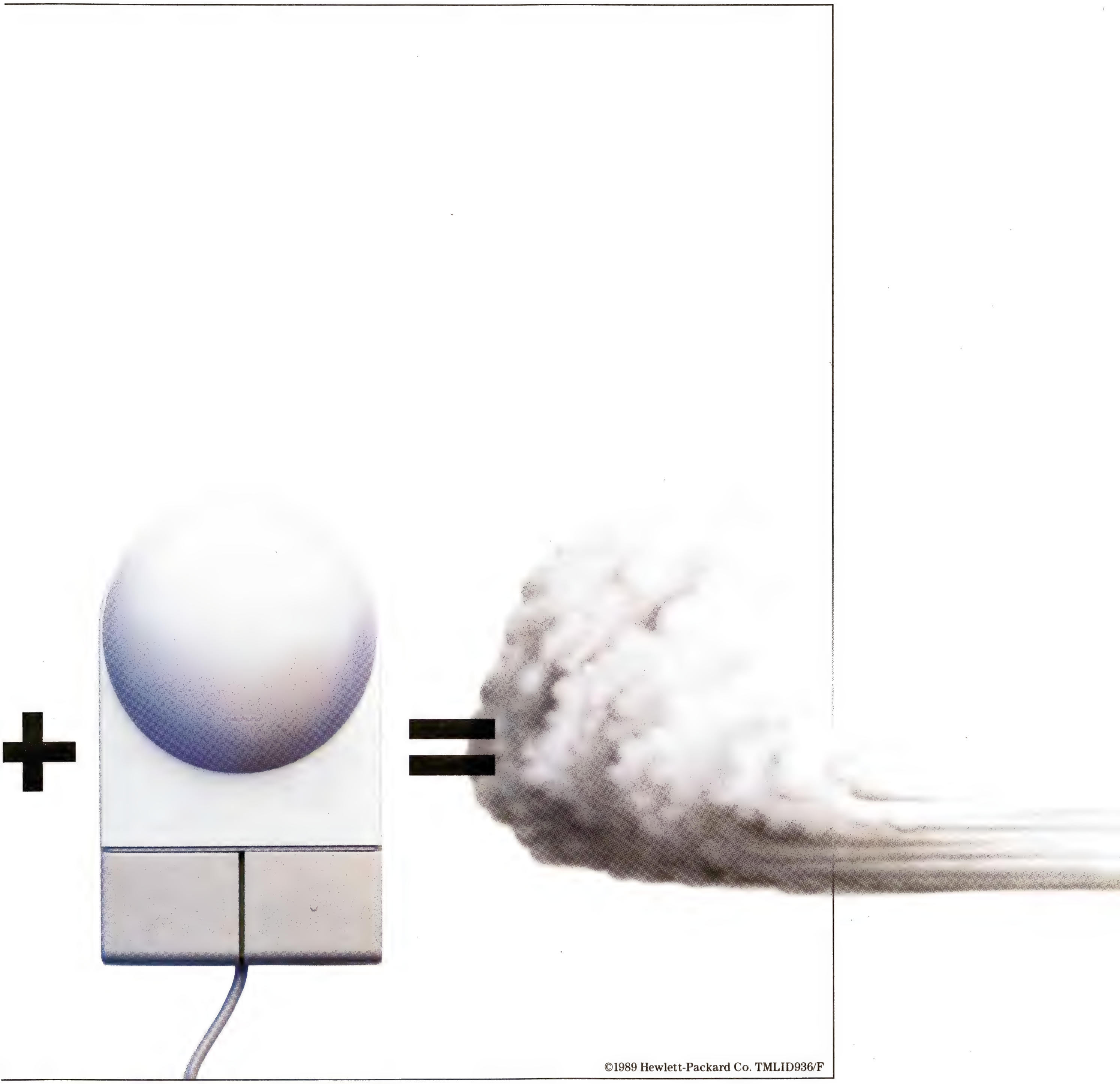

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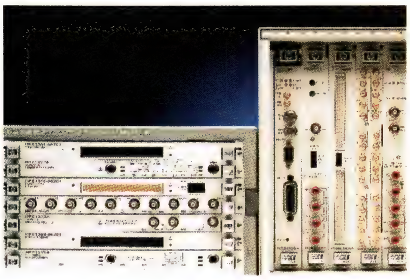

*The HP 75000 VXI is part of HP's Measurement System Architecture.

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CIRCLE NO. 52

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

SINGLE-BOARD COMPUTER COMBINES 16-BIT µP AND FORTH

Take a Motorola 68000 µP and combine it with 64k bytes of battery-backed RAM; a battery-backed real-time clock; parallel ports for a printer, a keypad, and an LCD; two serial ports (one a multidrop RS-485); and an extended 32-bit version of the Forth-83 development environment burned into ROM, and you have the $295 SBC68K single-board computer from Vesta Technology Inc (Wheatridge, CO, (303) 422-8088). The board measures 8×4 in. and requires 650 mA from a 5V power supply. You can plug as much as 128k bytes of RAM and 256k bytes of ROM into sockets on the board, which also incorporates an EPROM programmer.—Steven H Leibson

ETHERNET INTERFACE CONTROLLER FREES CPU POWER

The DP83932 systems-oriented network-interface controller (SONIC) from National Semiconductor (Santa Clara, CA, (408) 721-5000) frees your CPU from the drudgery of handling Ethernet messages. The DMA device includes an AUI-compatible analog-interface circuit and transmit and receive FIFO buffers. It also has a content-addressable memory that identifies, without CPU intervention, which incoming messages your system should receive. The controller can place incoming messages into system memory without CPU intervention and can transmit a string of messages from system memory with a single command. Multiple devices can share the same memory space, thus passing messages from one network to another without the CPU handling the message data. The device operates with system clocks as fast as 20 MHz and costs $55 (100).—Richard A Quinnell

MEMORY SYSTEM PROVIDES FORMAT CHOICES

Mass-storage systems from Hewlett-Packard (Palo Alto, CA, (800) 752-0900) can integrate a 5¼-in. 332M-byte or 664M-byte hard-disk drive with two additional drives of your choice. You can choose among DAT (digital-audiotape) drives that can back up 1.3G bytes of data in two hours; CD-ROM drives with access to 600M-byte data disks; rewritable-optical-disk drives that conform to the ISO and ANSI definitions for the continuous-composite format and whose cartridges can store 650M bytes of data; or additional hard-disk drives. All these drives communicate via a SCSI, are supported on the HP 9000 Series 300 workstations, and fit into two full-height 5¼-in. slots. The costs of the systems range from $4975 for a system with the 332M-byte hard-disk drive and two empty slots to $21,475 for a system with three 664M-byte hard-disk drives.—Michael C Markowitz

PRINTER OFFERS BRAILLE FONTS

A modified version of Howtek's (Hudson, NH, (603) 882-5200) Pixelmaster color ink-jet printer prints raised graphics and braille fonts to provide tactile communications for the visually impaired. Developed with the National Federation of the Blind, the printer uses a thermal ink jet to produce a raised dot on standard office paper. The ink is a plastic that the printer melts into a liquid; it solidifies when it comes in contact with the paper. A software program, which comes with the unit, translates the alphanumeric keys on the keyboard to braille fonts. The printer, which costs about $8000, also prints visual color graphics and text.—John Gallant

OP AMPS TAKE AIM AT VIDEO DESIGNS

Elantec (Milpitas, CA, (408) 945-1323) has announced several high-bandwidth op amps for video applications. The EL2423 quad 500-MHz op amp slews at 350V/μsec and draws 4 mA/amplifier. The op amp is stable for gains greater than 10. In a 14-pin plastic DIP, the part costs $14.24 (100). The EL2232 is a dual version of the EL2020; the device integrates two current-feedback amps with unity-gain bandwidths of 60 MHz for the same power as the EL2020. The amplifier operates from ±15V supplies, and its output swings ±12.5V into a 500Ω load. Other specifications include an offset voltage of 3 mV; a slew rate of 600V/μsec; and a 125-nsec 0.02% settling time to a 10V step. Prices start at $7.50 (100) for an 8-pin plastic DIP. Both op-amp packages include short-circuit protection.—Anne Watson Swager

CACHE RAMs OPERATE AS FAST AS 50 MHz

A family of cache RAMs is available from Logic Devices (Sunnyvale, CA, (408) 720-8630). The family comprises 16 devices: three cache-tag memories, six 16k-bit static RAMs (SRAMs), and seven 64k-bit SRAMs. The cache-tag memories have 4k×4-bit (L7C180/181) or 8k×8-bit (L7C174) organizations. They signal a cache hit within 10 nsec. You can use these devices in parallel to accommodate wider addresses and wire-OR their match-output lines.

The SRAMs are available in 1-, 4-, and 8-bit-wide organizations. The 16k×1- (L7C167), 4k×4- (L7C168, L7C170/1/2), and 2k×8-bit (L6116) memories have access times of 10 nsec. These memories, coupled with a 10-nsec tag RAM, let your cache system operate as fast as 50 MHz. The 64k×1- (L7C187) and 16k×4-bit (L7C161/2, L7C164/5/6) memories have access times of 12 nsec; the 8k×8-bit (L7C185) memory has an access time of 15 nsec. These devices are available in a variety of package styles, including DIPs and surface-mount packages. Cache-tag RAMs cost from $44.50 (100), and SRAMs cost from $14.65 (100).—Richard A Quinnell

MEETING TO COVER SBCs AND REAL-TIME OPERATING SYSTEMS

DSP Associates (Newton, MA, (617) 964-3817) will hold a conference on single-board computers for a variety of bus architectures and real-time operating systems. The East Coast meeting will be March 5 to 8 at the Massachusetts Institute of Technology in Cambridge, MA; the West Coast meeting will be May 14 to 17 at Rickey's Hyatt Hotel in Palo Alto, CA. Participating companies will include Motorola's Microcomputer Div, Intel Corp, Force Computers, SBE Inc, and Wind River Systems. For more information, phone Alexander Chelminsky at (617) 964-3817. You can reach him by fax at 617-969-6689.—Julie Anne Schofield

DESKTOP-ENGINEERING CENTER OFFERS CLASSES

You can use many general-purpose PC-based software packages, such as spreadsheets and database managers, for scientific and engineering applications if you know the right tricks. Binary Engineering (Waltham, MA, (617) 290-5900) recently opened its Center for Desktop Engineering Training to help you learn some of those tricks. The center's next class, which will be taught February 6 to 7, is "Engineering Design and Analysis Using Lotus 1-2-3." Registration for the class costs $695. The company will bring its classes to your site for approximately $3500 plus travel expenses.—Steven H Leibson

TMC2310 Runs 1024-Point FFT in 0.5ms

Here's the FFT runner you need to win the race. It's the TMC2310 — the first single-chip FFT controller to be this fast and simple to use.

Imagine all of these capabilities on one chip: Arithmetic functions, FFT coefficients ("twiddle factors"), even built-in address generation. That's why the TMC2310 runs forward or inverse transformations, or multiple equal-length FFTs totalling 1024 points, in just 0.5ms. Or a complex radix-2 butterfly in only 100ns. The TMC2310 executes other functions just as quickly, including FIR filtering and vector operations. Even data windowing is included without impact on either performance or price.

Better still, no development system is required. The TMC2310 jumps into action with just two 13-bit control words. It's so simple. No complex, bit-slice, microcode-intensive building blocks. No chip sets to contend with either.

You can qualify for a FREE sample. Just tell us about your application and we'll send you a TMC2310 to run in your system. You can build a complete spectrum analyzer with the TMC2310, our new 12-bit ADC (THC1200 Series), our TDC1012 DAC and external data and window memories. Be a winner. Try the TMC2310. Available now in 88-pin plastic pin grid array (PPGA) from TRW LSI Products or your nearest Hall-Mark or Hamilton/Avnet location.

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CIRCLE NO. 53

NEWS BREAKS

CONTRACTOR DEVELOPING REAL-TIME, DISTRIBUTED OS

Concurrent Computer Corp (Tinton Falls, NJ, (201) 758-7000) is under contract to the Air Force to develop a real-time, distributed operating system. The Alpha operating system will become part of the public domain upon completion. This extremely ambitious project, if completed successfully, will link virtually any computer system running any one of a number of common operating systems. Written in C++, Alpha will use the FDDI fiber-optic link as its backplane as well as support other common networks.

Concurrent seeks to form a consortium to promulgate Alpha. Research and Development Director E Douglas Jensen and Marketing Director William Blundon will answer any questions and provide any level of technical information in response to serious inquiries. Jensen forewarns that many basic real-time-system practices do not scale up to a distributed real-time system.—Charles H Small

SOFTWARE EXTENDS PC BUS ANALYZER ABILITIES

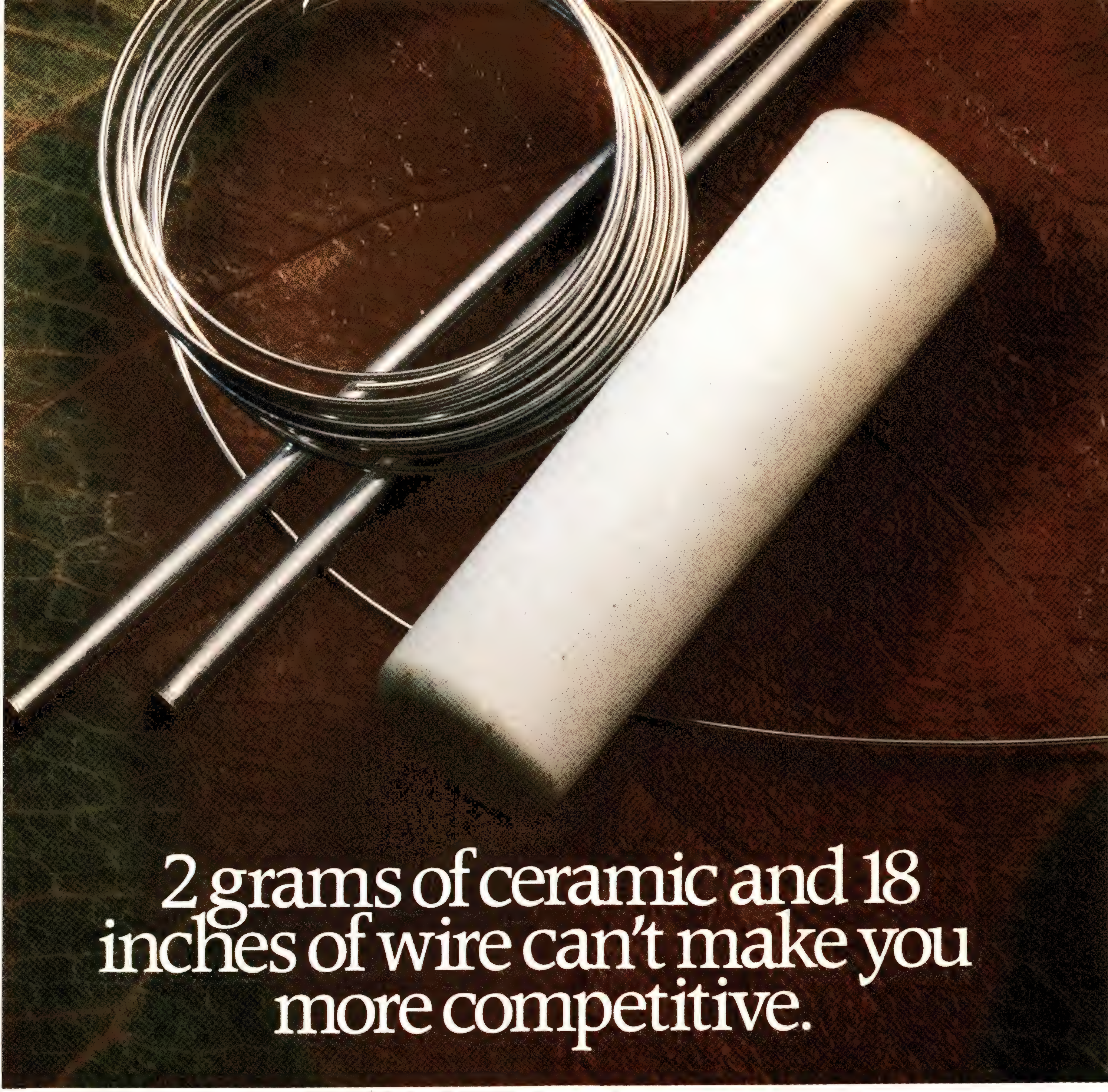
Release 2.60 of the AT BusTrak bus-analyzer software from Applied Physics Inc (West Lafayette, IN, (317) 497-1718) enables the company's IBM PC/XT/AT bus analyzer to disassemble captured trace files for both 8- and 16-bit μPs and display histograms showing bus utilization. Further, a validation filter eliminates invalid bus transfers from waveform displays. Present owners of bus analyzers that are still covered by the company's warranty can obtain the new software for free. The bus analyzer with the new software costs $1995.—Steven H Leibson

FLASH A/D CONVERTER CAPTURES PULSE PEAKS

An 8-bit variant of the standard full-parallel flash converter captures the peak amplitude of square pulses without an additional peak-hold circuit. TRW LSI Products' (La Jolla, CA, (619) 457-1000) TDC1035 peak digitizer captures the maximum amplitude of one or more input pulses occurring between asynchronous reset pulses. For pulse widths of 30 nsec and greater, the converter digitizes peaks to its full dc linearity, which is ½ LSB. The IC can also detect pulses as narrow as 12 nsec, although at this pulse width the converter underestimates the pulse's amplitude by about 15%. The digitization accuracy of any pulse's peak value depends on the shape of the pulse; the manufacturer characterized this ADC using square pulses with controlled rise and fall times of 8 nsec. You can estimate the device's performance with other pulse shapes by using an energy-above-threshold model. The 24-pin ceramic IC consumes 1W and includes an output register with 3-state outputs. All digital input and outputs are TTL compatible. Commercial and military versions of the part cost $19 and $95 (1000), respectively.—Anne Watson Swager

BUSCON SESSION TO HIGHLIGHT BUS ANALYSIS

A new session at Buscon/90-West—to be held on February 14 to 16 at the Long Beach Convention Center, CA—will explore some of the issues surrounding the use of bus analyzers. Speakers at session 503, "Applying Bus Analysis Tools in a Real-Time Development Environment," will address bus-analysis problems on IBM PC bus, NuBus, VMEbus, and Multibus systems. For more information about the convention, phone (203) 852-0500, ext 247.—Steven H Leibson



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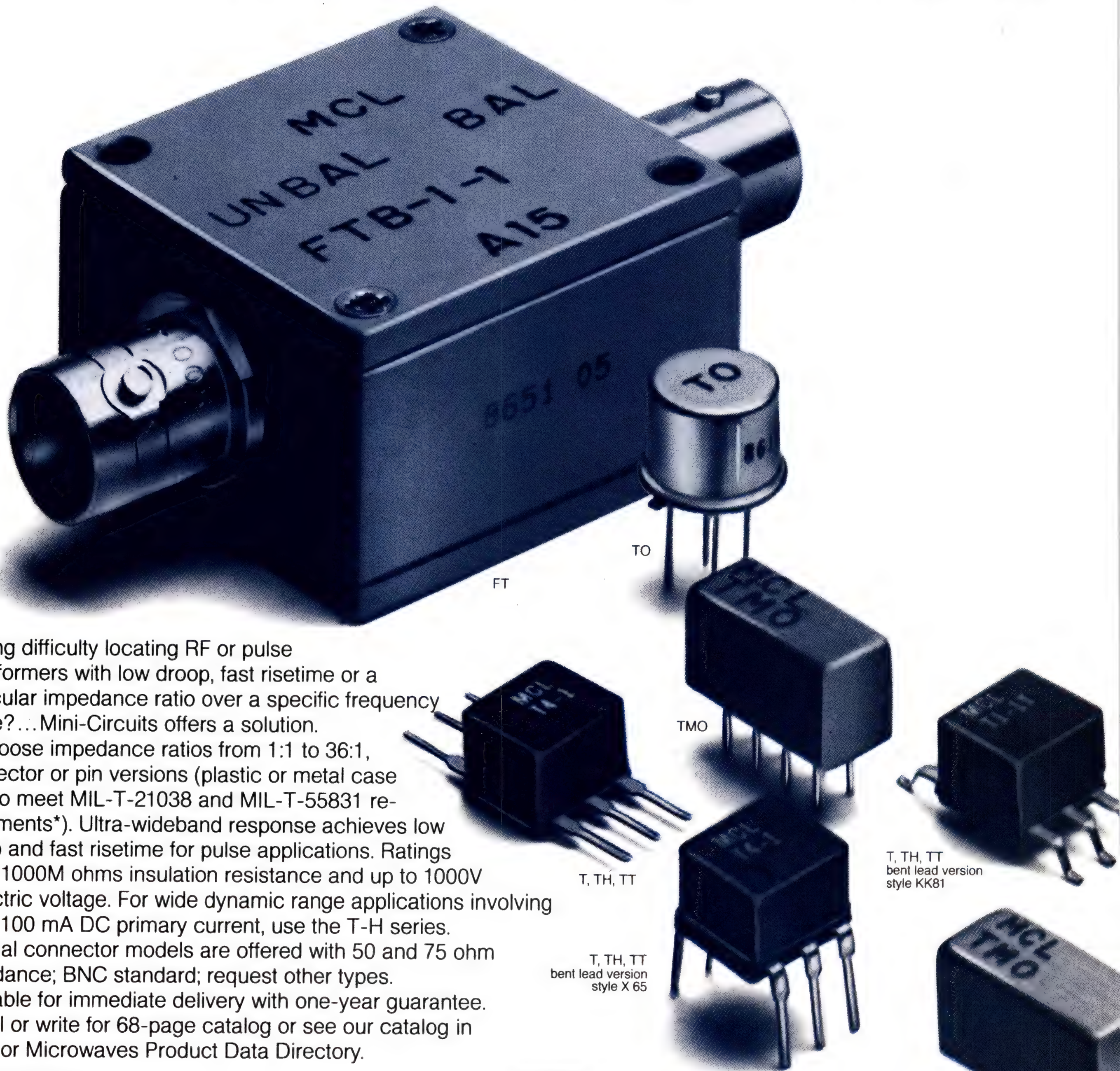

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case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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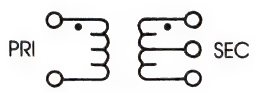
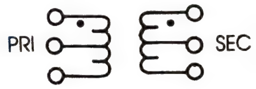
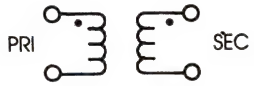
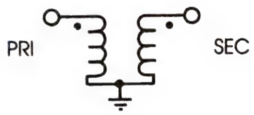
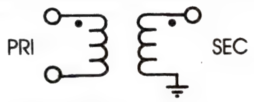
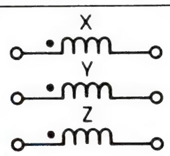
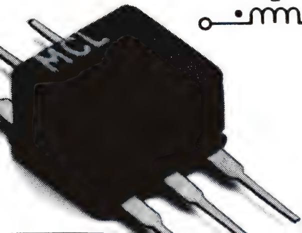
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



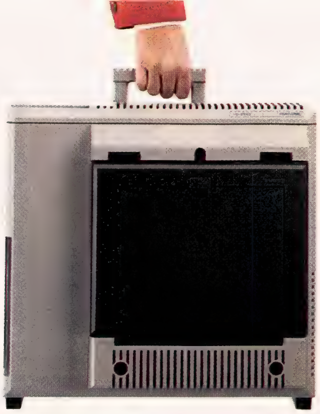
■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS
Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

CIRCLE NO. 55

HIGH-SPEED HARDWARE ANALYSIS MODULES: THE NEWEST PAYOFF TO YOUR PRISM INVESTMENT.



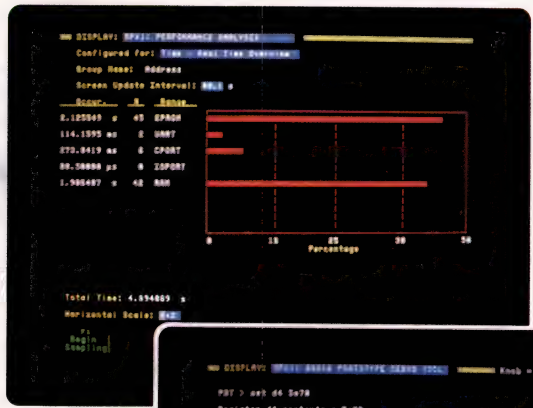
Visualize a logic analyzer that not only acquires microprocessor state and timing data, but adds emulation capabilities... real-time performance analysis... high-speed timing for hardware analysis... and more—all usable in precise, time-correlated combination. All configurable to your needs.

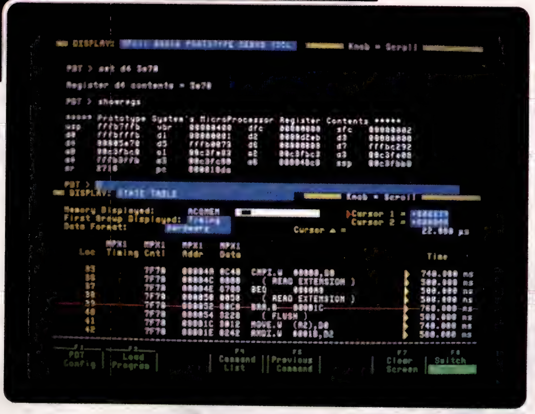
That's the visible edge of the Prism 3000 Series from Tektronix.

The new dimension of integrated analysis.

MPM/MPX Module	Microprocessor control Real-time performance analysis 200 MHz hardware analysis 8K deep state analysis Multiple Microprocessor support
HSM Module	2 GHz hardware analysis 300 MHz state analysis 1.5 ns glitch capture 12K transitionally-stored memory (up to 120K effective memory)

Now, just months after introduction, Prism breaks *new* barriers with a module specifically designed for hardware analysis—for detecting glitches, metastability, and the other common problems of state machines, busses, and sequential logic.

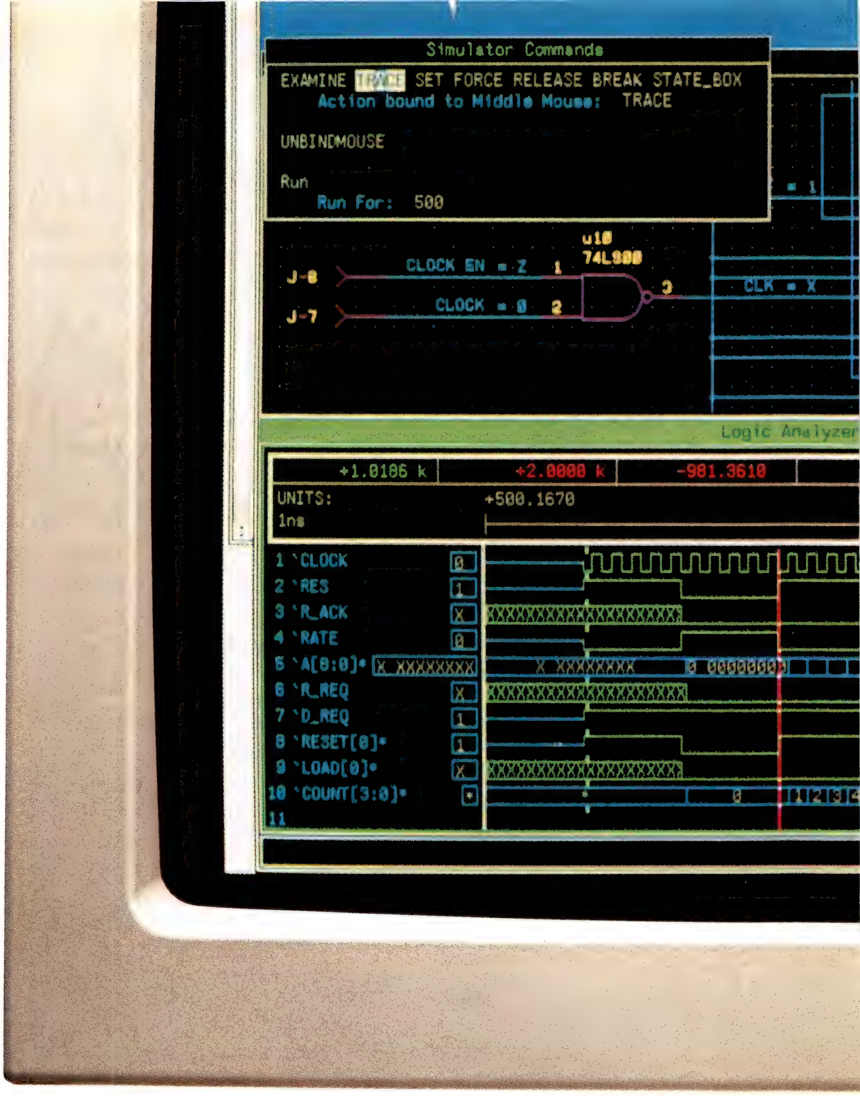




Start with up to 96 channels and the exceptional resources of Prism's 8/16/32-bit microprocessor integration modules.

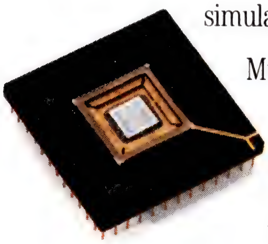
You can view 200 MHz timing and 8K of state data per channel,

(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.



CAE for people to see how their

If your CAE tools are telling you too little too late, consider this news from Teradyne. Now you can capture and analyze complex ASIC and VLSI board designs with unprecedented accuracy and ease, using our Vanguard™ schematic entry software and LASAR simulator in Teradyne's MultiSim™ environment.



LASAR's accurate worst-case timing analysis means you won't be held up by faulty prototypes.

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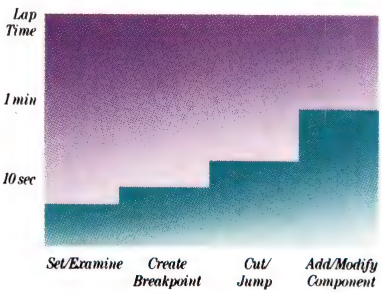

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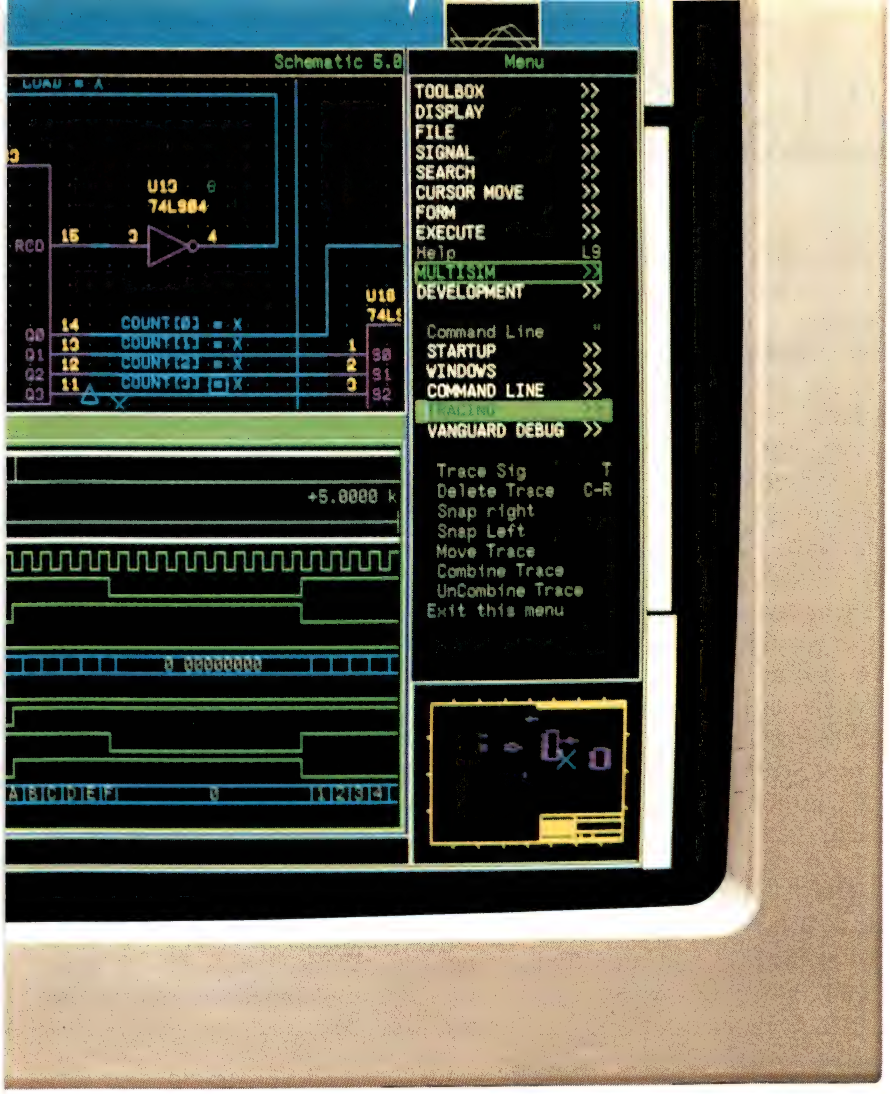

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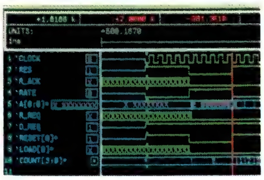

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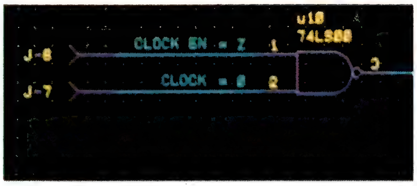

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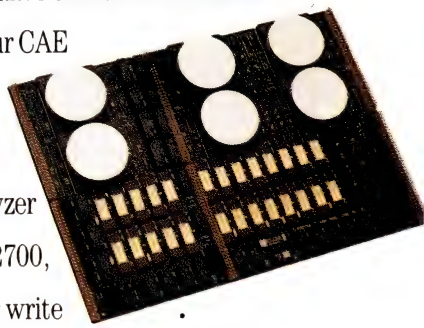

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CIRCLE NO. 56

Bob Pease sends corrections

Thank you for printing my letter about ICs that are nonstandard (EDN, October 26, 1989, pg 33). However, the statement reading, "The following list of parts all share the same pinout" contains an error. It should read, "The following list of parts all *have a nonstandard* pinout.

An error also crept into **Fig 1**, Part 12 of the series on troubleshooting analog circuits (EDN, October 26, 1989, pg 176). VA does connect to two diodes and to R_2, but VA does not connect to the op-amp input. Therefore, this path should be broken. Similarly, the bottom of R_2 does not connect to ground, but it does connect to the input of the amplifier.

Finally, in Part 11 of the series (EDN, October 12, 1989, pg 177), the original text of a statement in the lower left column read: "...features as good a temperature coefficient as you'd probably ever be willing to pay for." I realize the EDN Stylebook frowns on using "good" in statements about specifications, so the editors changed it to "high." Unfortunately, "good" in this case means "low." The sentence should read: "These bandgap references feature as low a temperature coefficient as you'd probably ever be willing to pay for."

Robert Pease
Staff Scientist
National Semiconductor
Santa Clara, CA

Tell them "We won't take it anymore"

Yes, I'm mad as hell. Jon Titus's editorial "She'll be right, mate" (EDN, October 12, 1989, pg 49) touches on a problem that I find more and more unsettling as time goes by. From busboy to president, everybody relies on a "Santa Claus" to make things right. Worse yet, without a "Santa," Americans are getting ever more helpless. Recently, the TV show, "Hidden Video," set up a phony Canadian border crossing outside a California desert town and made people swear to uphold the laws of Canada. I find it very hard to visualize one of the Founding Fathers falling for such a prank.

What has turned a proud, self-reliant nation into a bunch of nitwits that needs to be told what to do and not to do every step of the way? Not only responsibility seems to have vanished, but common sense as well. While one might construe the "Don't blame me!" syndrome as

Beveled Glass Window by Thomas Tisch & Andreas Lehmann Oakland, California

merely a side effect of the pursuit of happiness, what can account for the simultaneous urge to become victims?

Could the Founding Fathers have unwittingly built a time bomb? The Constitution was constructed to safeguard against arbitrary rule by an aristocracy, an oligarchy, or any other elite. By setting up a government "not of men, but of laws," the framers may have planted a dangerous seed: The guardians of these laws would eventually usurp the power of the people to rule themselves.

It's taken 200 years for the seed to grow into a clear and present danger, but today there can be little doubt that many of us live in daily fear, not of law, but of lawyers, much as earlier civilizations trembled in fear of their High Priests. "The law" has been turned into a monster that only the Anointed can understand and keep at bay—after adequate sacrifices. We have by now been trained to seek our lawyer's blessing not just before embarking on any journey, but also upon returning. If anything went awry, he'll tell us who was "at fault" and how to cash in on every mishap.

Innovators, producers, and their sponsors have become prime targets for the modern witch hunters. Naturally, the litigators line their pockets with the wealth that should have benefited our industries' (and the country's) growth. The message "Don't take chances" pervades our business world. A clique of unproductive tea-leaf readers, pretending to "make her right, mate," is paralyzing progress and goading the nation into a mindless stupor.

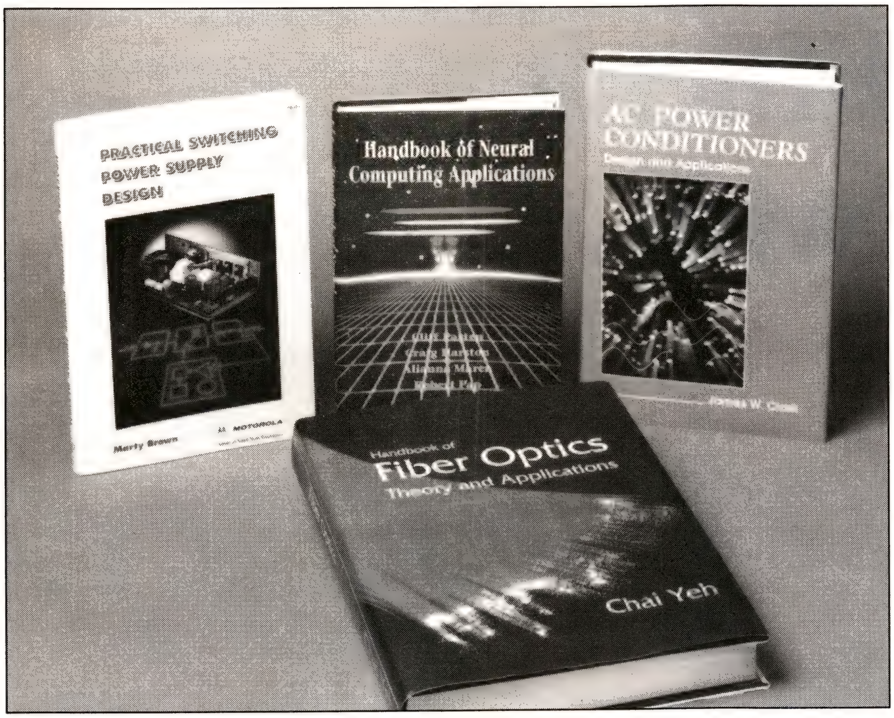
What can we, as innovators and as citizens, do to break the spell? We must tell our legislators in no uncertain terms, "We're mad as hell, and we won't take it anymore." If we yell loud enough, they might listen—at least the few who aren't lawyers.

Max J Schindler
Prime Technology
Boonton, NJ

Correct phone number and location

In the Technology Update (EDN, October 26, 1989, pg 115) entitled "CAD tools aren't yet on speaking terms," two errors appear in the **box** on pg 116. The phone number for Honeywell Systems Inc should be (612) 782-7322, and the company is located in Minneapolis, MN, rather than in Boston, MA.

High Performance Reading



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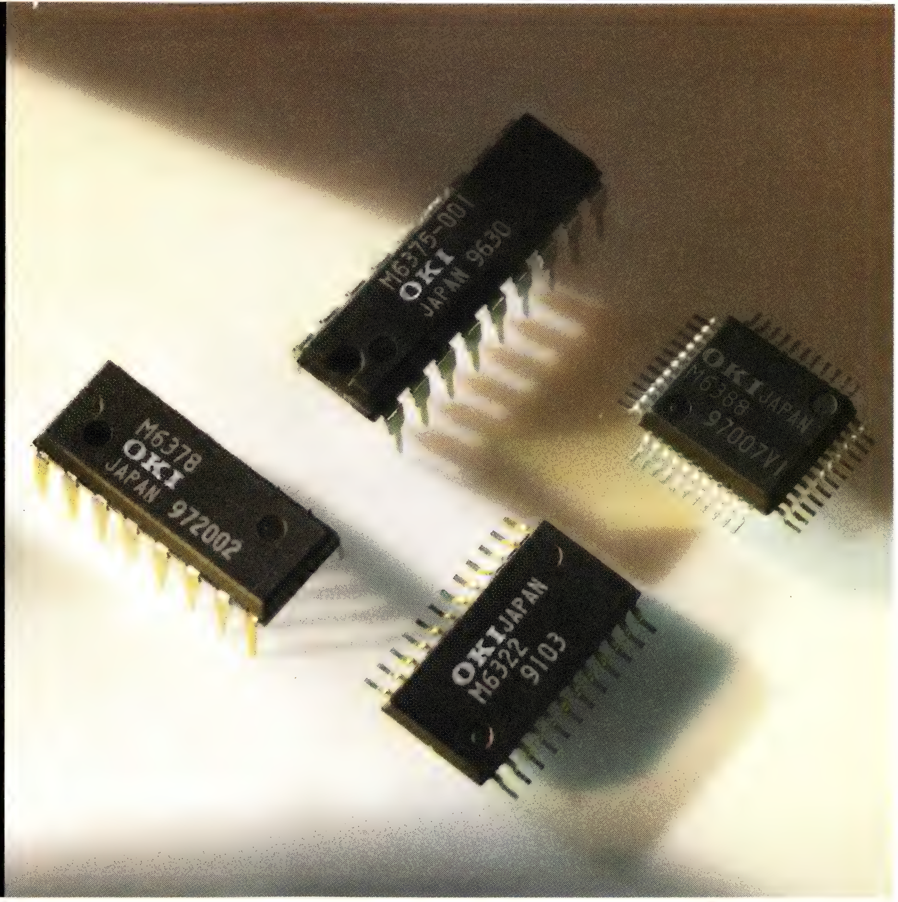

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Winter 1990 UNIX Technical Conference, Washington, DC. Judith DesHarnais, USENIX Conference Office, 22672 Lambert St, Suite 613, El Toro, CA 92630. (714) 588-8649. January 22 to 26.

SaudiComputer '90, Saudi Arabia. Gerald G Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. January 28 to February 1.

SEMICON/Southwest, Dallas, TX. Semiconductor Equipment and Materials International, Shows Dept, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 964-5111. January 31 to February 1.

SECS Communications Seminar, Dallas, TX. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. February 2.

1990 6th IEEE/CHMT Semiconductor Thermal & Temperature Measurement Symposium, Scottsdale, AZ. C/S Communications, Box 23899, Tempe, AZ 85285. (602) 967-7444. February 4 to 8.

2nd International Tape Automated Bonding (TAB) Symposium, San Jose, CA. Dr Subash Khadpe, Semiconductor Technology Center, Box 38, Neffs, PA 18065. (215) 799-0919. FAX 215-799-2677. February 5 to 7.

Communication Networks '90, Washington, DC. IDG Conference Management Group, Box 9171, 20 Speen St, Framingham, MA 01701. (508) 879-6700. February 5 to 8.

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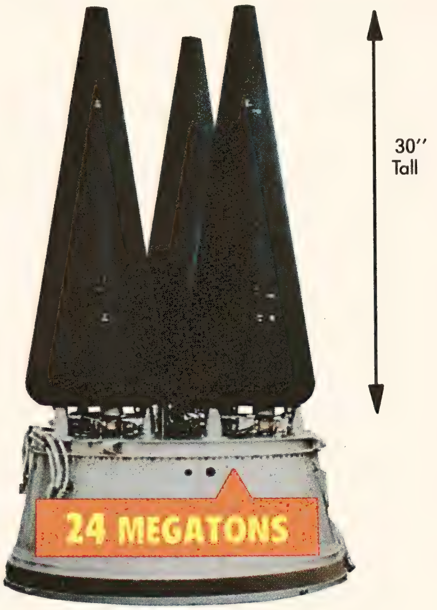

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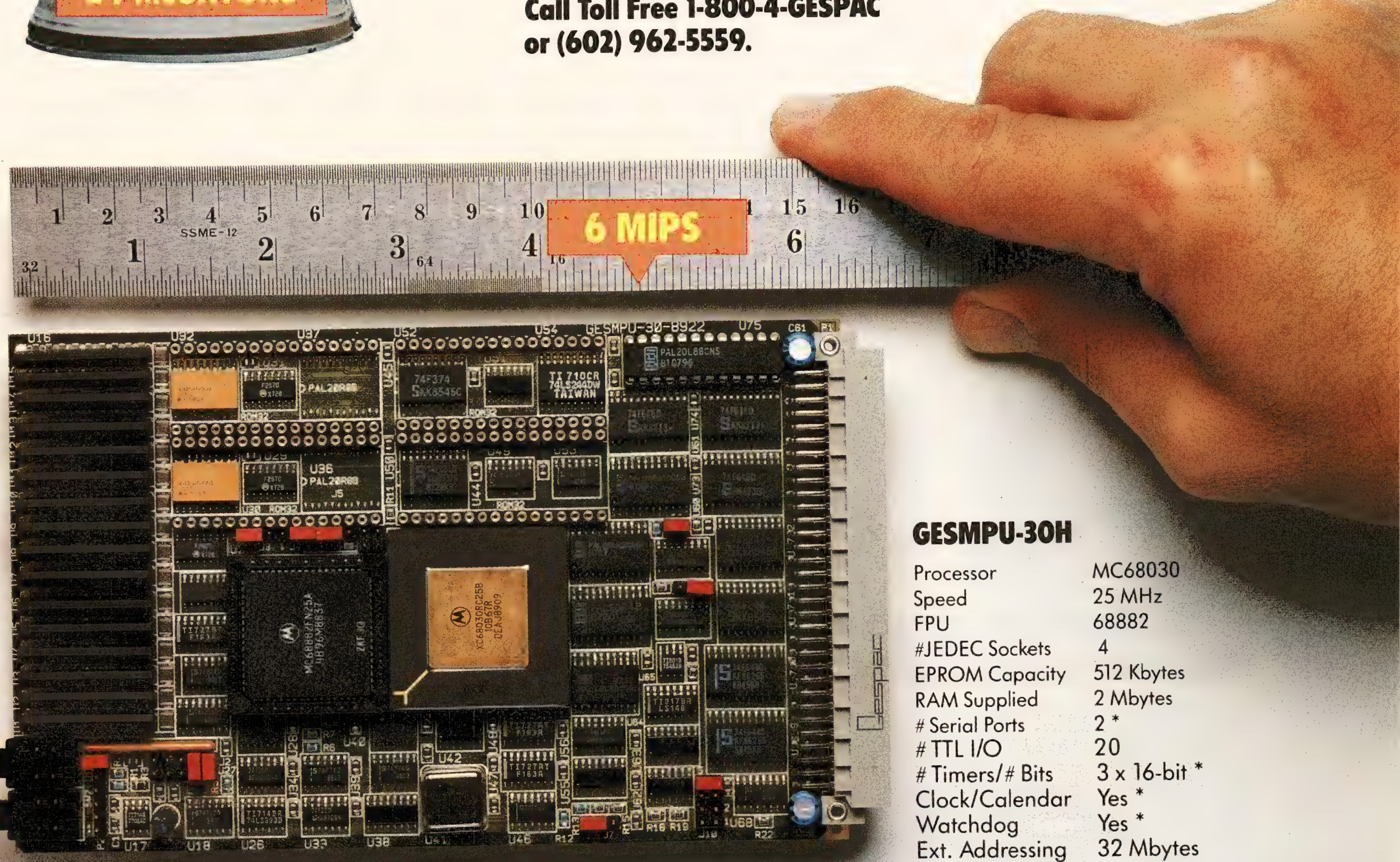

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CIRCLE NO. 58

CALENDAR

Hands-on UNIX for Programmers (short course), Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. FAX 206-527-2806. February 7 to 9.

1990 Symposium on Electronic Imaging: Science and Technology/Exhibit, Santa Clara, CA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. February 11 to 16.

IEEE Instrumentation and Measurement Technology Conference, San Jose, CA. Robert Myers, IEEE Instrumentation and Measurement Society and IEEE Santa Clara Valley Section, 3685 Motor Ave, Suite 240, Los Angeles, CA 90034. (213) 287-1463. FAX 213-287-1851. February 13 to 15.

Systems/USA, San Jose, CA. Chuck Jungi, American Electronics Association, 5201 Great America Pkwy, Santa Clara, CA 95054. (408) 987-4204. February 13 to 15.

Buscon West, Long Beach, CA. Sharon Salvo, Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500, ext 253. February 14 to 16.

Modern Power Conversion Design Techniques (short course), San Diego, CA. Joy Bloom, Bloom Associates Inc, Educational Div, 115 Duran Dr, San Rafael, CA 94903. (415) 492-1239. FAX 415-492-1239. February 19 to 23.

SECS Communications Seminar, San Jose, CA. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. February 26.

Electronic Imaging West, Pasedena, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. February 27 to March 1.

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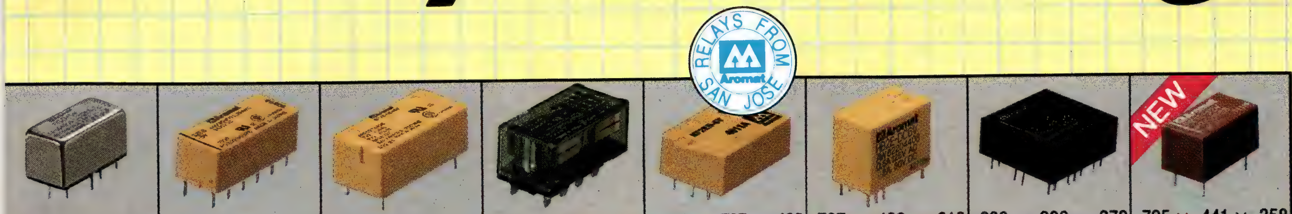

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10^6	10^5	10^5	10^5	10^6	2×10^5	10^5	3×10^5
10^9	10^8	10^7	5×10^7	(2C) 3×10^8 (4C) 10^8	10^7	5×10^6	5×10^6
1000Vrms	1500Vrms	3750Vrms	3000Vrms	1000Vrms	1000Vrms	2000Vrms	1000Vrms
—	—	—	—	1500V FCC	—	—	—
(DC) 5, 6, 12, 24, 48V	(DC) 5, 6, 12, 24, 48V	(DC) 3, 5, 6, 12, 24, 48V	(DC) 3, 5, 6, 12, 24, 48V	(DC) 5, 6, 12, 24, 48V	(DC) 3, 5, 6, 12, 24, 48V	(DC) 3, 5, 6, 9, 12, 24, 48V	(DC) 3, 5, 6, 9, 12, 24V
(Single) 150mW (–L) 70mW (–L2) 150mW	192 to 355mW	240mW	300mW	(2C) 300mW (4C) 480mW	(1C) 360mW (2C) 580mW	(Single) 350-400mW (–L) 180-200mW (–L2) 350-400mW	(Single) 200mW (–L) 200mW (–L2) 400mW
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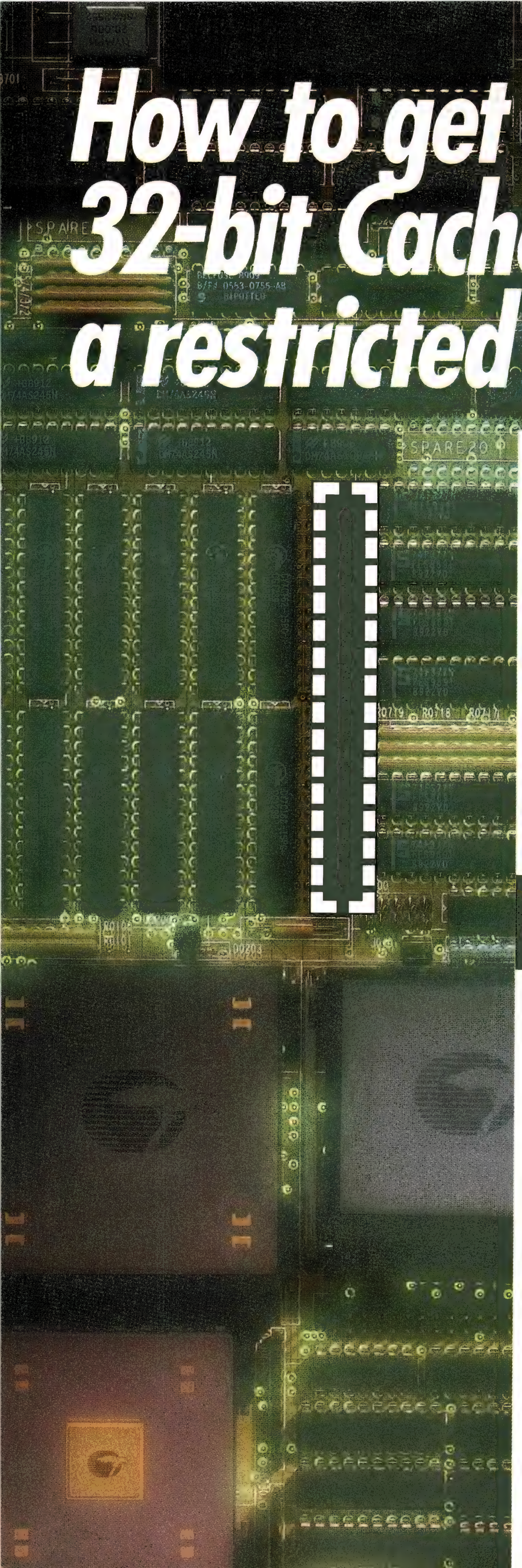

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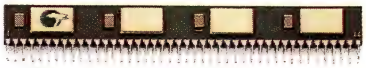

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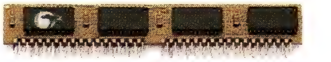

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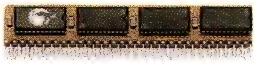

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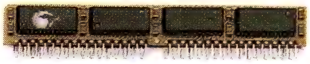

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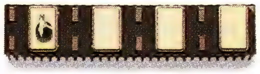

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People often ask, though, what is innovation? Isn't it something more than simply developing new things? In truth, yes. Not every new product is an innovation, nor is every engineer an innovator. To me, the heart of innovation is imagination and the ideas that spring from it. No one can be an innovator without having—and using—a fertile imagination, for without one you cannot see the future and how to reach it.

If you want to be an innovator, start using your imagination right now. Conjure images of

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- a company that has no managers, only leaders who champion and sponsor people and ideas
- a company that promotes and encourages entrepreneurial spin-offs and new ventures and developments when it can't exploit them itself
- a business that encourages people to pursue ideas and to make intellectual leaps—even though they might sometimes fail.
- an enterprise in which engineers aren't stuffed into a Black Hole of Calcutta to do "engineering," but are encouraged to help set market, service, and product-definition goals
- a venture that does less market research and decides to "just do it" and get the market's reaction to a real product
- a company that encourages or demands that people think of what they can do, rather than what they cannot
- a firm that encourages employees to use their imaginations.

Forming images is the easy part. But, to become truly innovative, you must put your ideas and the ideas of others into action. You must try to bring the future up to the present. You'll never be an innovator unless you set *real* goals and strive to reach them.

Jon Titus

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CIRCLE NO. 60

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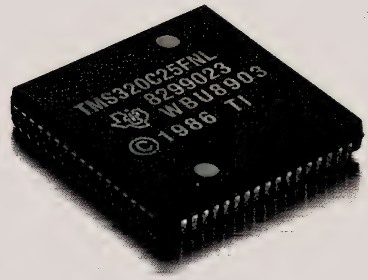

The TMS320C25.

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03,*–. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

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[1] EDN, "EDN's DSP Benchmarks," September 29, 1988.

Measuring the cost of quality: German engineering at the crossroads

Article and photographs by Gary Legg,
Special Projects Editor

This article is the first in an occasional series about engineering in Europe.

On the Autobahn, traveling from Munich to Regensburg at 170 kilometers an hour, you get a feeling for what German quality is all about. Even at that high speed, the BMW rumbles softly like a large, lithe cat. When a sudden stop is necessary to avoid two cars that have been involved in an accident, braking is fast, smooth, and precise. Later, talking with engineers at Siemens AG, the international electronics giant whose headquarters are in Munich, the German attitude toward quality becomes apparent. It's more than respect; it's almost a reverence.

And yet, as markets become more global and more competitive, that attitude is changing. Increasingly, in order to remain competitive, German engineers speak of shortening product-development times. Again and again, though it seems to go against their nature, they mention "stopping the design" when it's "good enough" and of reducing component costs. More and more, they're concerned with lowering overall costs. Their challenge, of course, is to reduce costs while still keeping quality at an acceptable level. And for a German, "acceptable level" means "high."

Quality—or reliability, at least—isn't even negotiable for Dr Alfons Härtl. Group leader of airbag electronics for Siemens at the company's automotive-electronics division in Regensburg, Härtl explains that an airbag must fully inflate in 30 milliseconds during an accident, and then it must quickly deflate. The bag must work perfectly when it's needed, and it must never inflate when it's not needed. Still, Härtl says, airbag prices must come down. The use of passive restraints—either airbags or special seat belts—has been mandated for cars sold in the US beginning with 1990 models. Airbags produced in high volumes are potentially cheaper than passive seat belts, and because several major companies are supplying airbag systems, price competition will be fierce.

For Dr Anfons Härtl, group leader of airbag electronics at Siemens AG, product quality isn't negotiable. In many car accidents, airbag deployment can mean the difference between life and death.

In the US, Härtl continues, manufacturing volumes are much higher in the automotive industry (and thus in the automotive-electronics industry) than in Europe. Consequently, reducing the price of each individual component is important. "They stop the design," he says of some US engineers, "before [German engineers] would say it is finished. There are some [US] products on the market that we would not normally accept." To be competitive, he says, German engineers now have to "reconsider in our minds the design of such products if we want to have success in the US market. We have to think differently and figure out how to stop a design a little bit earlier and bring a product to market in the right time and at the right price."

Giuliano Visintini, a researcher for Siemens in Munich, concurs with Härtl's assessment of German versus American quality. A native Italian who attended the Technische Universität Wien (Technical University of Vienna) in Austria and is pursuing a doctorate there, Vis-

intini has visited a number of American companies on two trips to the US. "In the US," he says, "engineers are able to get acceptable quality in a very fast time and at a low cost, and then they start something new. In Germany, we work longer and try to get better quality, but at the same time we increase the cost."

Surface-acoustic-wave (SAW) devices, for which Visintini develops simulation models, illustrate his point. Siemens makes superior SAW devices, the researcher says, but they compete with products from other companies that are cheaper. In many companies, he says, "production cost is the first thing and quality is second."

But it isn't simply a desire to keep improving a product that fosters German quality. Often, improvements occur simply as a result of continued, long-term involvement by individuals. Because German engineers change jobs less often than their American counterparts, they frequently have more opportunities to apply their understanding and insight to improvements. On the average, German engineers work for only three employers during an entire career.

In his observations of US companies and engineers, Visintini has noticed what he feels is a detrimental effect of personnel changes on quality. Viable approaches to problems often get discarded in favor of new approaches, he says, simply because a person who best understands an approach leaves for a new job. "If you're in a company for only two years," Visintini says, "you need the first year to understand what your problem is and the second year to solve it. If you stay a third year, you can make improvements, but if you go somewhere else, you can't." Engineers tend to stay at Siemens a long time, Visintini notes; he and his colleagues are able to use and improve software that was first developed 10 years ago, because some of its original developers still work there.

Giuliano Visintini, an Italian who studied at the University of Vienna, now works for Siemens in Munich developing simulation models for surface-acoustic-wave (SAW) devices. German engineers' concerns for quality, Visintini notes, often result in high development costs.

Another factor that encourages quality work, according to Härtl, is that employees at German companies expand their responsibilities across defined job boundaries. Because boundaries between engineering jobs in Germany tend to be blurred, he says, an individual engineer is apt to tackle any problem that becomes apparent, even if it's nominally someone else's problem. At an American aerospace company with which he worked closely for three years as a supplier, Härtl observed just the opposite. There, he says, "Everyone looks for a well defined position and defines his boundaries. When a problem falls between boundaries, no one takes care of it unless it becomes very visible."

To Wolf Jaenecke, a Siemens project manager for telephone switching systems, quality stems from a basic attitude. The US is market driven, he says, and Germany is quality driven. "Sometimes," Jaenecke comments, "Germans and Americans just don't understand each other."

The difference in outlook became apparent to Jaenecke a few months ago during an in-house seminar for cross-cultural training. In one of the seminar's exercises, Siemens engineers were divided into an American team and a German team and instructed to develop marketing plans for a fictional "fitness monitor," a device to be worn on the wrist like a watch. The German plan resulted in an expensive, high-quality product whose technical merits were to be heralded in advertisements in upscale magazines; the American plan, in contrast, called for an inexpensive product to be sold in discount stores.

The German and American teams even worked in different ways. The Germans' first activity was to organize their team, determining who would lead it and then deciding who would work on each of the tasks. Once they had established a structure, the team members worked individually. The Americans, on the other hand, hardly bothered with structure or individual tasks; their marketing plan was almost entirely the result of brainstorming.

Structure with flexibility

At Siemens, weekly meetings that last from two hours to half a day are obligatory as you move up the chain of engineering management. At lower levels, meetings are less likely to be required, but they're still fairly common. Nevertheless, Jaenecke believes that in one sense, at least, German managers are less rigid than Americans. American managers, he says, sometimes exert undue pressure on

American dream, German reality: a 37½-hour work week and six weeks or more of annual vacation.

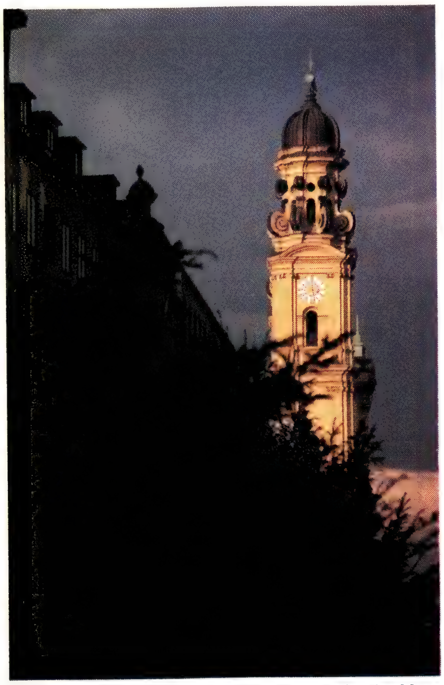
schedules to get a product to market on time. In general, however, Jaenecke gives American managers high marks; within American organizations that he has observed, he has admired the clear lines of reporting, the strong group identity, and the overall friendly, casual work atmosphere.

Härtl, who supervises half a dozen or so engineers and is "about 50% engineer" himself, seems anything but rigidly structured. Gregarious and energetic (he was an avid sky diver and hang glider before marriage and children), he favors unscheduled, day-to-day contact over formal meetings. "For me," he says, "it's important to have good relations with the engineers." Härtl also stresses the importance of listening to the engineers' ideas and not forcing his own upon them. The notion that "we're going to do this—no discussion—is the past. It's no longer working."

What does work in Germany, in sharp contrast with the US, is a strong engineers' union. Union achievements, in fact, may contribute to the much praised German technical quality; with a standard 37½-hour work week and six weeks or more of vacation each year, few engineers are likely to be burned out on the job. Not all German engineers belong to a union, but those who do can't be forced to work more than a certain number of hours per day (usually 10) or to work an excessive number of overtime hours per month (usually 20). In some cases, the union may agree to additional overtime, but engineers either get paid extra or get additional vacation time for their efforts. At Siemens, engineers can earn as much as 10 additional vacation days per year for working overtime, thus accruing a total of eight weeks.

Often, however, German engineers donate a certain amount of overtime out of expediency. In most cases, they can receive extra pay or vacation time only if they apply in the preceding month, so in short-term crunches, they may work some additional time without extra pay. Many engineers, especially those who are young and ambitious, may also work overtime voluntarily to advance their projects. At Siemens' Regensburg automotive-electronics division, for example, many engineers have only two or three years of experience. "They want to solve problems," says Härtl. "All you have to do is give them some guidance so that they work in a common direction."

Most German engineers, in fact, are accustomed to being self starters, because their university education requires them to be. A student must pass an examination to get a diploma, but the education program is remarkably unstructured. Attendance isn't required at lectures, for example, and a professor probably won't even notice a student's absence. There aren't even required textbooks. Härtl, who undertook some graduate study at the State University of New York at Albany, was amazed that exams there were based on specified pages of specified books.



Spire of the 17th-century Theatinerbirche in Munich, located near the headquarters of Siemens.

Assessing a new Europe

The flexibility that is so evident in German education, and which appears to be reflected in companies such as Siemens, may be the key to the future for German electronics companies. West Germany is already the dominant economic power in Europe, and it's poised to increase its commercial standing through opportunities that are now appearing in a realigned Eastern Europe. Nevertheless, the country's electronics industry faces a continual struggle against larger American and Japanese industries. And even though the united Europe of 1992 will make pan-European trading easier for its members, the resulting common market will also create opportunities for non-European companies.

Many Japanese companies in particular are well prepared for the changing European marketplace. Long accustomed to selling abroad, they have been quietly gearing up for a post-1992 Europe. Even the one area where German industry has long reigned supreme now faces a Japanese threat: New luxury cars from Japan are competing directly against the classic Mercedes and BMW.

A major problem the Germans face, and one that they fully recognize, is that the Japanese are able to produce quality that's "good enough" (or better) at an attractive price. Although many German engineers dispute the notion of Japanese quality being equal to German, they concede that it's nevertheless

high and, more significantly, less expensive to produce.

Still, old attitudes die hard. Pride makes it difficult to design a product that's just "good enough" when the traditional design goal has always been "the best." But if engineers at Siemens are typical of those throughout the German electronics industry, then a new attitude is emerging that could make the difference between a future of growth and one of decline.

Quality will remain high, according to the new attitude, and the old reverence for quality certainly won't disappear. Most German engineers will probably continue to strive for quality that's more than just "good enough." The difference now is that, to be more competitive, they may have to settle for less than perfect. EDN

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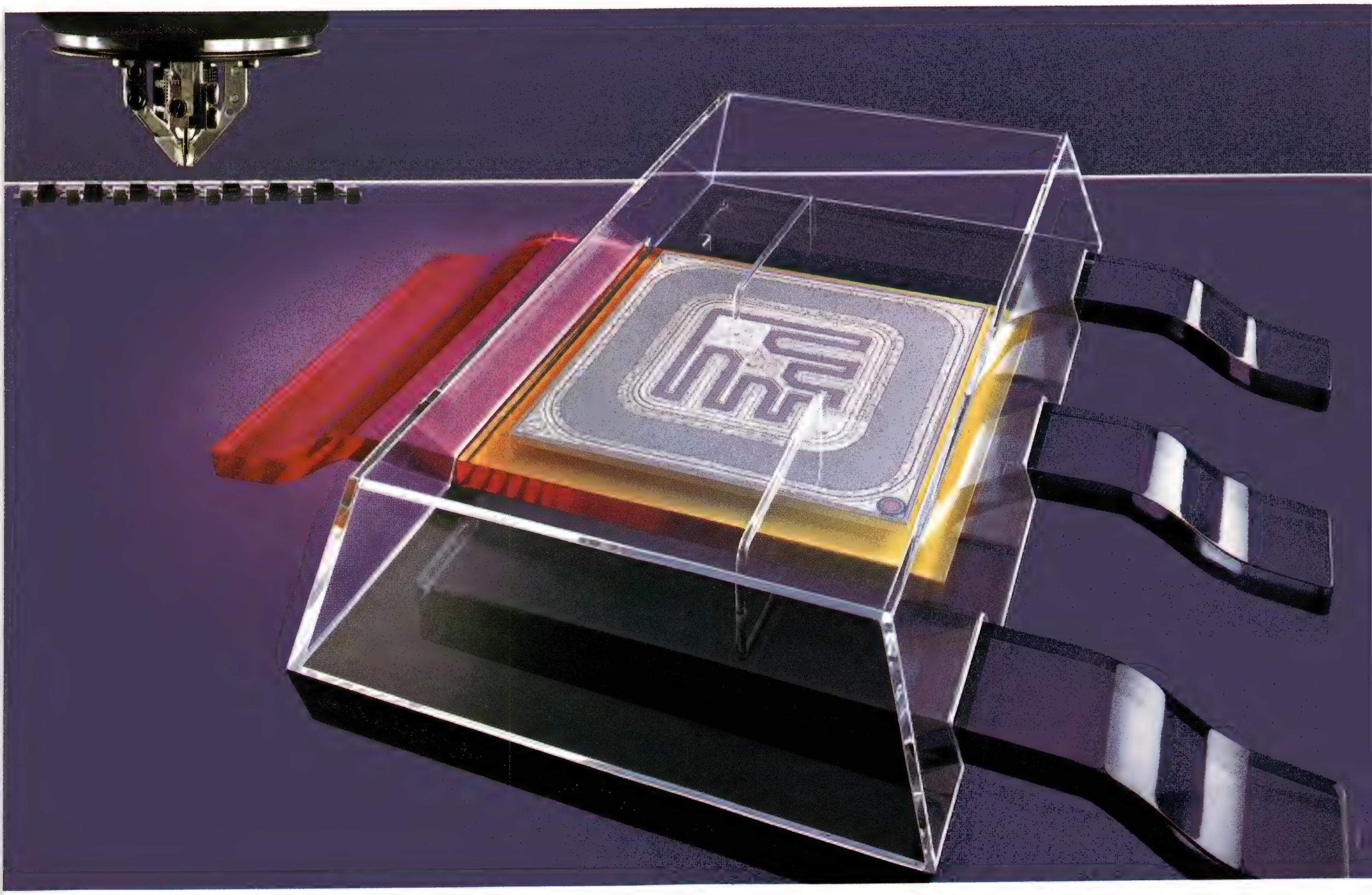
WHAT'S COMING IN EDN

EDN Magazine's February 1, 1990, issue will feature a staff-written Special Report on how add-on buses let you attach small I/O boards to your computer at low cost. Part 3 of the designer's guide to flash-ADC testing concludes this design series with a discussion of the measurements you'll need to fully characterize flash A/D converters. Also, Contributing Editor Bill Travis looks at analog comparators that address TTL and ECL ICs.

Remember to look for our regular departments, and in EDN's February 15 issue, look for coverage of static RAMs.

SIEMENS



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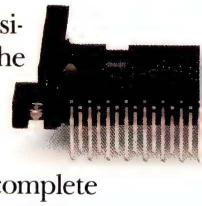

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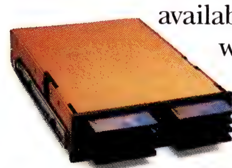

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CIRCLE NO. 35

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TOKEN-RING BOARDS

Standard efficiently allocates channel use

Expect token-ring LANs to become popular beyond IBM installations as designers take advantage of the technical benefits they offer compared with Ethernet networks.

Maury Wright,
Regional Editor

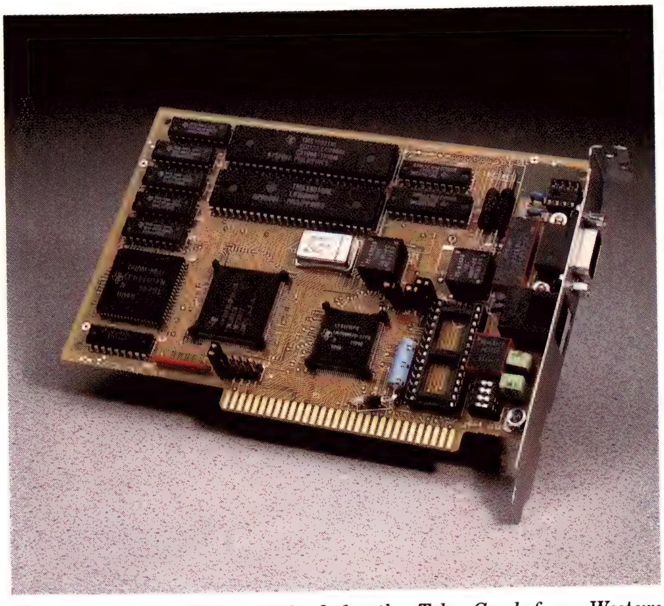
LANs based on the IEEE 802.5 token-ring standard offer system designers a way to implement an extremely reliable network with a guaranteed allocation of network bandwidth to each node. Furthermore, signal collisions on busy networks do not degrade the bandwidth of token-ring LANs. However, most people use the token-ring standard because it is IBM's network of choice. Outside of IBM installations, Ethernet LANs are more popular for office-automation applications. But expect to see more token-ring LANs in nonIBM installations.

Six months ago only a few manufacturers offered token-ring boards for IBM-compatible PCs. After Comdex, the number of manufacturers tripled. Likewise, more companies now offer token-ring cabling systems and multistation access units (MAUs), or wiring centers. Companies have also begun offering token-ring boards for architectures other than the IBM PC/AT and Microchannel Architecture (MCA) buses.

Token-ring LANs transmit data at 4M or 16M bps, but products that support the faster rate are just emerging. The availability of faster token-ring boards will serve to further boost the popularity of the network.

Token-ring- and Ethernet-based LANs differ only at the physical- and data-link layers of the ISO's 7-layer OSI model. For more information on the basics of the token-ring standard, see **box,** "The token-ring standard—IEEE 802.5," and **Ref 1**. Popular network protocols such as TCP/IP (Transmission Control Protocol/Internet Protocol), TOP (Technical and Office Protocol), NetBIOS, and the evolving ISO protocols run on token-ring, Ethernet, and other physical- and data-link layers.

The Ethernet technique offers a maximum data-transfer rate of 10M bps but employs a CSMA/CD (carrier sense multiple access with collision detection) scheme to allocate network bandwidth. In a heavily loaded network, collisions waste network bandwidth and, there-



Shielded cable is not required *for the TokenCard from Western Digital to achieve its 4M-bps transfer rate. The card is compatible with popular network software such as Netware and NetBIOS.*

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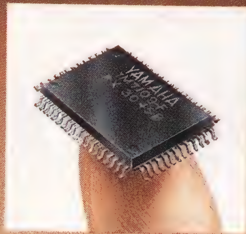

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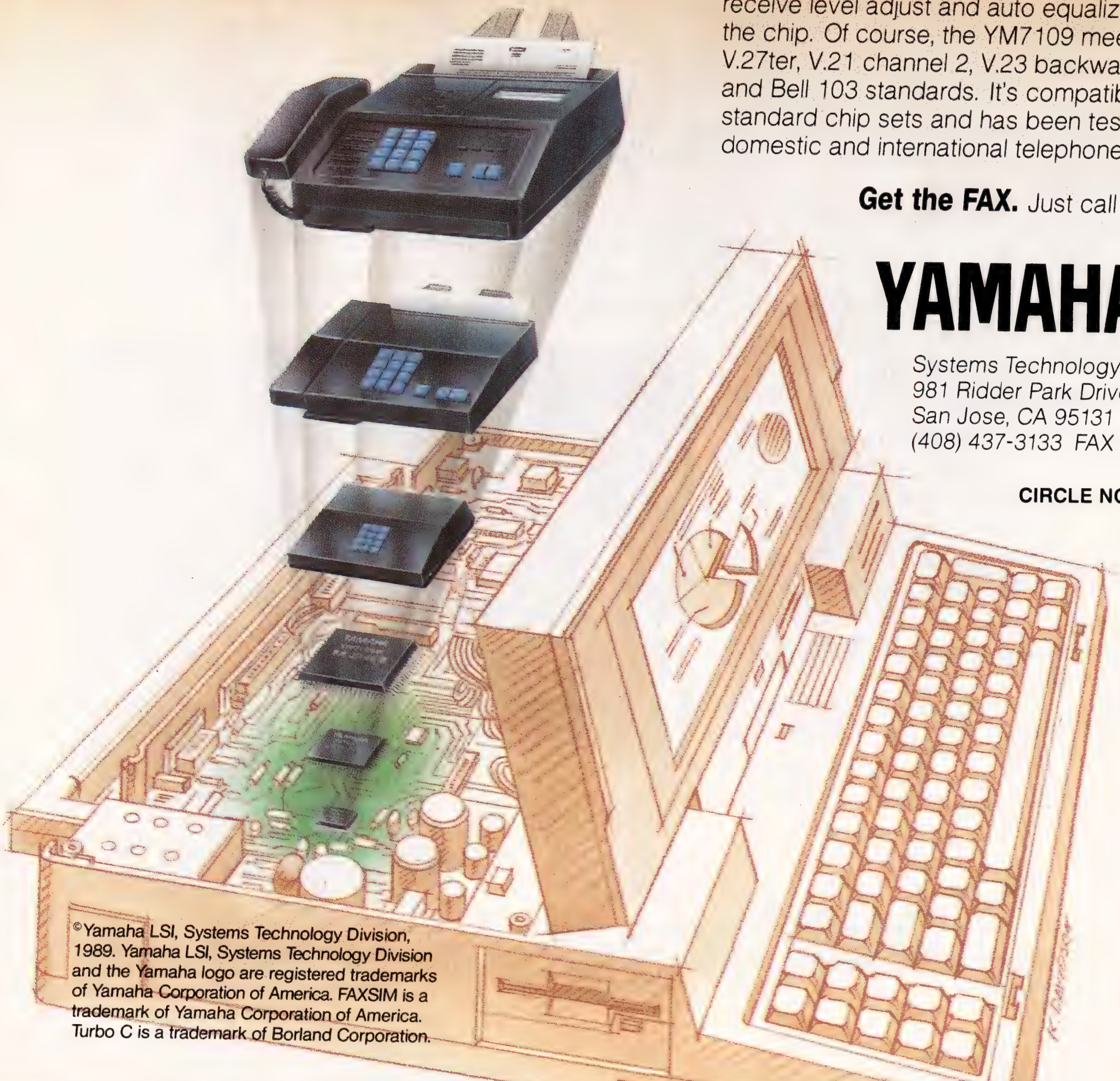


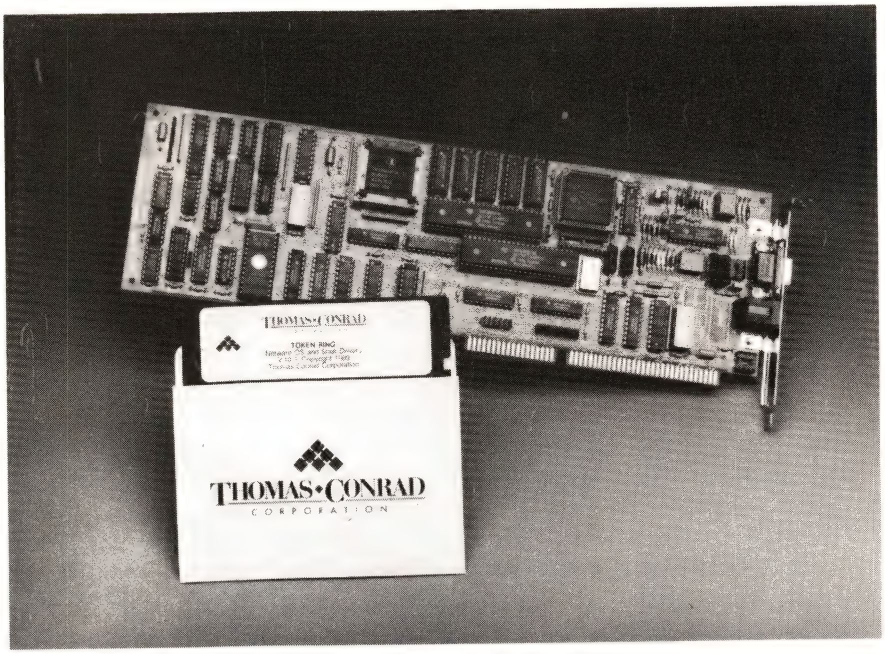
805-A-004-89

fore, reduce efficiency. The token-ring technique guarantees bandwidth for priority transmissions and, based on its implementation, can fairly allocate bandwidth to all nodes.

In a heavily loaded network application, token-ring networks approach 100% efficiency. Each consecutive node captures the token in turn, and only overhead in the token, addressing, and status bytes wastes bandwidth. Conversely, on a LAN with sparse traffic, the Ethernet technique offers the advantage of immediate access to the channel. Expect to see 16M-bps token-ring LANs providing high-speed backbones between departmental Ethernet LANs due to the different operational characteristics of the two techniques.

The token-ring technique also offers advantages in reliability and maintenance compared with the Ethernet technique. Ethernet LANs employ either bused coaxial cable to connect nodes in a bus wiring scheme or a star-configured twisted-pair medium with active hubs. The bused connections make the initial installation simple but make maintaining and changing the wiring and diagnosing problems difficult.

Token-ring LANs typically employ a star configuration with passive hubs, commonly called MAUs. You can isolate any node on a token-ring network by unplugging a cable or throwing a switch in the wiring closet. Likewise, you can isolate one MAU from a network and therefore isolate a group of nodes for testing. An MAU and the token-ring cabling scheme also let the network self-heal. Relays in MAUs and on interface cards and the shorting connectors used on MAUs and cables automatically eliminate problems with powered-down stations or disconnected cables.



***The bus-master capability** built into Thomas Conrad's TC4035 token-ring card speeds data transfers across the host IBM PC/AT-compatible bus.*

Token-ring interface cards should cost less than Ethernet cards. The Ethernet interface requires a digital component to both transmit and receive data and an analog component to detect collisions. A token-ring interface only requires a digital receive and a digital transmit component. The popularity and volume of Ethernet parts, however, make them less costly. A token-ring board for a personal computer typically costs 50 to 100% more than an Ethernet board.

Until recently, you had only a few products to choose from to implement token-ring LANs. IBM offers this LAN for all its system products. In addition, IBM offers its Token-Ring Adapter II ($650) for IBM PC/XT- and PC/AT-compatible systems and the Token-Ring Adapter II/A ($750) for MCA-based systems. These boards only support 4M-bps token-ring operation. The Token-Ring Adapter II only transfers data across the host bus in 8-bit increments. Neither product offers bus-master capabilities.

These boards are compatible with IBM's LAN Manager and the NetBIOS transport protocol. They use a 9-pin DB-type connector, and you can use shielded or unshielded dual twisted-pair cable with them. IBM also offers a 4-channel token-ring MAU that costs $727 and occupies a 1¾-in.-high space in a 19-in. rack. The IBM MAU includes connectors that short automatically when disconnected.

Western Digital offers lower-priced alternatives to the IBM products. The TokenCard WS costs $499, includes a 3k-byte static-RAM buffer, and suits applications in NetBIOS or Novell (Provo, UT) Netware workstations. Western Digital also offers the TokenCard, which it recommends for servers and all IBM software environments. It costs $599 and includes the features of the TokenCard WS as well as a 128k-byte dynamic-RAM buffer and local protocol store. Both cards offer an 8-bit host interface. The cards include both a 9-pin connector and an RJ-11 phone interface.

Gateway Communications also offers lower-priced alternatives to

Token-ring boards

IBM products. The company offers an 8-bit IBM PC-compatible card for $595 and a 16-bit IBM PC/AT card for $695. The cards include both connector types and support Netware and NetBIOS.

Racore Computer Products offers an 8-bit token-ring board for only $399. The company also offers a 16-bit IBM PC/AT board and an MCA board for $499 each. You can specify a $70 18k-byte buffer that supports the downloading of protocol software as an option.

Bus masters speed DMA

Recent announcements centering around boards that support 16M-bps operation and the host-bus-master capability also promise to spur interest in token-ring LANs. Both features will let system designers take advantage of the performance potential of token-ring networks. Proteon has an IBM PC/AT card that can act as a bus master; several other companies have similar new products.

The IBM PC/AT bus has no provision for bus masters to arbitrate for the bus, but a bus master can take over the bus and perform DMA transfers independently of the mother-board DMA controller. This technique, often called first-party DMA, increases the effective

The token-ring standard—IEEE 802.5

IEEE 802.5 defines a LAN based on token passing and a physical ring that connects the nodes of the network. Each node can only access the network communication channel while holding the token. Therefore, this LAN automatically implements a guaranteed channel-access allocation scheme. This LAN also happens to be the network that IBM offers across its line of computer systems.

The token-ring standard deals with the lowest two layers—the physical layer and the data-link layer—of the ISO OSI model. The physical layer of a network includes connectors, cables, and the transmission of raw bits of data. The data-link layer ensures that the basic transmission facility is free of errors. The medium-access-control (MAC) sublayer corresponds to the upper portion of the physical layer and lower portion of the data-link layer.

Above the MAC sublayer, the token-ring network is compatible with the popular Ethernet (IEEE 802.3) network and with the token bus (IEEE 802.4) used in manufacturing-automation-protocol (MAP) LANs. Token-ring LANs encode data using a differential Manchester scheme and employ twisted-pair wiring. Most installed token-ring LANs transmit data at 4M bps, but expect the newer 16M-bps addition to the standard to grow in popularity.

Token propagates around ring

A 3-byte token circulates around a token-ring LAN. Each LAN node retransmits all bits received with a 1-bit delay. A node captures the token by inverting a bit in the second byte of a free token. The first two bytes of the token then become a start-of-frame sequence. A station that captures the token follows the start-of-frame bytes with addressing information, a data frame or frames, check-sum bytes, an ending delimiter byte, and a frame-status byte. The node that captures the token and transmits data removes the data bits after they propagate around the ring.

The token-holding time parameter, typically 10 msec, specifies the length of time any node can hold the token. Only the token-holding time limits the size of frames transmitted, and a node can transmit multiple short frames in one token-holding time. After completing a data transfer, the station holding the token places a new token on the ring.

A priority field in the middle byte of the token can prioritize frames. An inactive node must wait to capture the token until the priority of the frame waiting for transmission is higher than the frame priority set in the rotating token. During retransmission, any node can set the priority field in the active token, providing that the node sets the field to a higher-priority status than the token previously held. Thus, the node holding the highest-priority frame reserves the next free token. A station that raises the priority of a token and captures it must lower the priority again when it is done. A system designer can set up a network with a completely fair allocation scheme or one that allocates a large part of the network bandwidth to high-priority traffic.

One node on the LAN acts as a monitor station and supervises the ring, thus setting up a centralized maintenance facility. The monitor ensures that the token isn't lost, handles problems with garbled frames, and drains the ring of orphan frames (frames left on the ring if a transmitting station loses power). On power up or after the failure of a monitor, a node assumes the role of monitor by issuing a claim-token control frame. All stations must be able to

bandwidth of the host bus. The potential for conflict exists, however, if you put several boards that can become bus masters in one system. Single-tasking MS DOS-based systems can typically operate with multiple bus-master cards.

Thomas Conrad Corp offers an IBM PC/AT-compatible board that supports bus mastering. The TC4035 board costs $595 and operates at 4M bps. It includes Netware and NetBIOS drivers and is compatible with IBM LAN software. You can also buy MAUs that support as many as 16 stations from Thomas Conrad. The company has reaffirmed its plans to offer a token-ring board for EISA systems, but has no time table to introduce such a product.

In the 16M-bps arena, IBM has been the first to ship products. The company offers the Token-Ring Network 4/16 Adapter for IBM PC/AT compatibles and the Token-Ring Network 4/16 Adapter/A for MCA-based systems. The boards cost $895 each and operate at 4M or 16M bps, but they do not have bus-master capabilities.

Although other companies have also introduced 16M-bps products, don't expect volume shipments of such products until about midyear because board manufacturers ha-

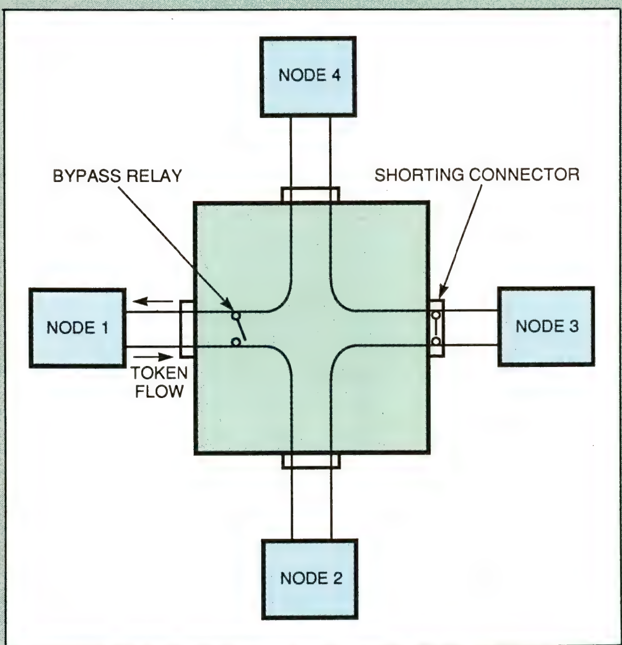


Fig A—An MAU offers fault tolerance *by including shorting connectors or relays that isolate a station that powers down. You can buy MAUs that include as many as 48 ports.*

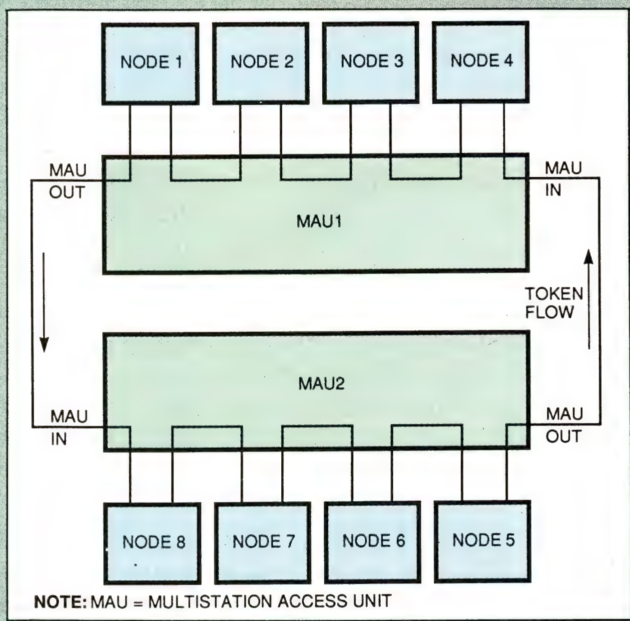


Fig B—MAUs form a physical ring *with input and output signals that connect to other units. You can isolate the subnetwork connected to any MAU with switches or by disconnecting the in and out cables.*

become monitors. A contention protocol sets up a new monitor if several nodes issue a claim token.

Figs A and **B** show typical token-ring wiring schemes. Most installations use a star configuration and wiring centers or MAUs (multistation access units) that connect stations. A single cable between an MAU and a station includes two twisted pairs to implement the ring. **Fig B** shows how to connect two or more MAUs.

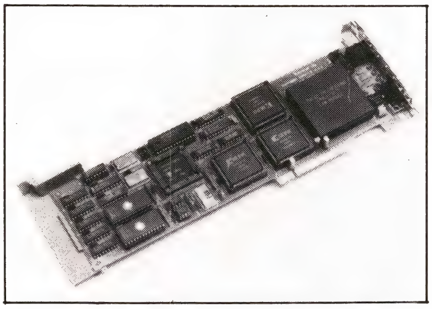
MAUs typically reside in wiring closets with phone equipment, and they increase the reliability and maintainability of token-ring LANs. MAUs are passive parts and, therefore, are only subject to the mechanical failures of relays, connectors, and wiring. The MAU shown in **Fig A** depicts two different ways to ensure reliability. Some MAUs include a relay dedicated to and powered by each station on the network. The relays bypass a station that is powered down or disconnected. Likewise, token-ring interface cards that reside in stations typically include a bypass relay to short input and output signals on power down. Some MAUs, including those offered by IBM, employ connectors that automatically short input and output signals when disconnected.

Token-ring boards

ven't been able to get token-ring chips. IBM developed a token-ring IC for 16M-bps operation and licensed Texas Instruments to manufacture the IC for sale to other board vendors. Texas Instruments, however, has met delays in producing the IC. The company recently pushed back the schedule for volume shipments until late this quarter. IBM builds its own chips, but virtually every other company's 16M-bps token-ring products use Texas Instruments' IC.

Manufacturers can soon expect other options for token-ring ICs. Toshiba America (Irvine, CA) introduced a 16M-bps IC and should have production volume about the same time Texas Instruments does. The Toshiba IC isn't compatible with Texas Instruments', but it will offer board manufacturers an alternative. In addition, Ungermann-Bass (Santa Clara, CA) offers a 16M-bps token-ring board based on a proprietary chip. However, the company only sells it as part of a bundled network system.

Proteon, Lantana Technology, Racore Computer Products, and Gateway Communications all recently introduced token-ring boards that support 16M-bps transfers. Furthermore, Western Digital and Thomas Conrad have made it clear that they are simply waiting for ICs before they announce similar products.



Microchannel Architecture-compatible token-ring cards *that offer bus-master capability combine with IBM PC/AT-compatible cards in Lantana Technology's Cypress family of token-ring products.*

Lantana Technology became the first company to introduce an MCA bus-master card for 4M-bps token-ring networks last year. The company recently introduced 16M-bps boards for the IBM PC/AT architecture and MCA. The boards should ship during the first half of the year. Proteon recently previewed EISA and MCA boards that run at 16M bps but has not announced pricing or availability.

Several recent announcements also point to the growing popularity of token-ring products outside the personal-computer market. Interphase now offers a token-ring board for VMEbus systems. The V/Token Ring 4212 Owl operates at 4M or 16M bps and costs $3595. The board includes a 68020 μP that manages the network interface. Furthermore, the board employs the MACSI (Multiple Active Command Software Interface) command interface, which all Interphase I/O boards use. MACSI simplifies the integration of token-ring LANs into systems that use other Interphase communication boards.

You can also buy token-ring interface boards for DEC Q-bus and BI-bus systems. Simpact offers hardware/software combinations that range from $7900 to $17,150. The boards support IBM's LAN protocols and TCP/IP.

Finally, MAU units are starting to go high tech. In the past, MAUs

For more information . . .

For more information on the token ring products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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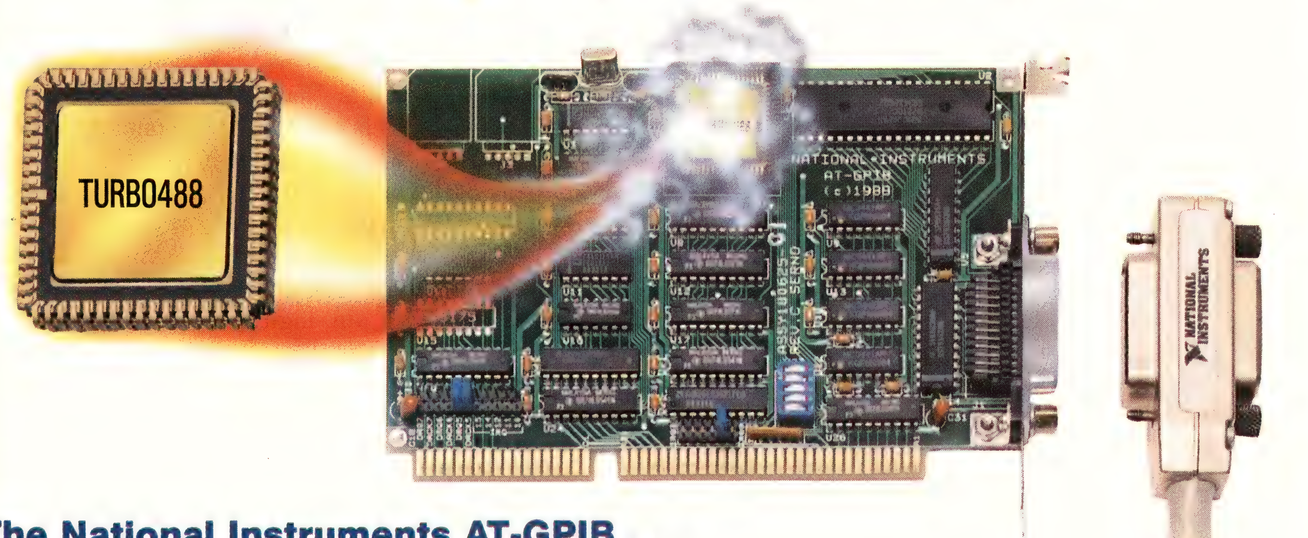

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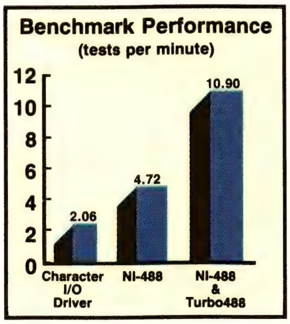

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Token-ring boards

included little more than connectors and wiring, but now you can buy units that have status LEDs and relays powered by connected nodes. Companies have also begun to offer units that surpass IBM's 4-node capability.

Mux Lab, for example, offers a 16-node unit that fits in the same 1$\frac{3}{4}$-in.-high rack as IBM's 4-node MAU. The company plans to add a 48-node unit that stands 3$\frac{1}{2}$-in. high by the end of the first quarter of this year. The 16-node device sells for $2590; the 48-node unit will cost $7500. The Mux Lab products include a shorting relay dedicated to each node and status LEDs. The units also have trunk-routing switches and employ RJ11 or RJ45 connectors.

IBM's products require shielded wiring for 16M-bps operation, but for $50 Mux Lab will sell you a signal conditioner that plugs into an IBM token-ring card and lets you use unshielded phone wire for 16M-bps needs. For customers who own IBM MAUs, the company offers signal conditioners for the interface between an MAU and an unshielded twisted-pair cable for $90.

Expect the companies that offer 16M-bps cards to include similar signal-conditioning capabilities. By midyear, such cards will be readily available for use with unshielded cable, and the token-ring alternative will emerge from its IBM shadow to claim its place as a legitimate choice for all office networks.

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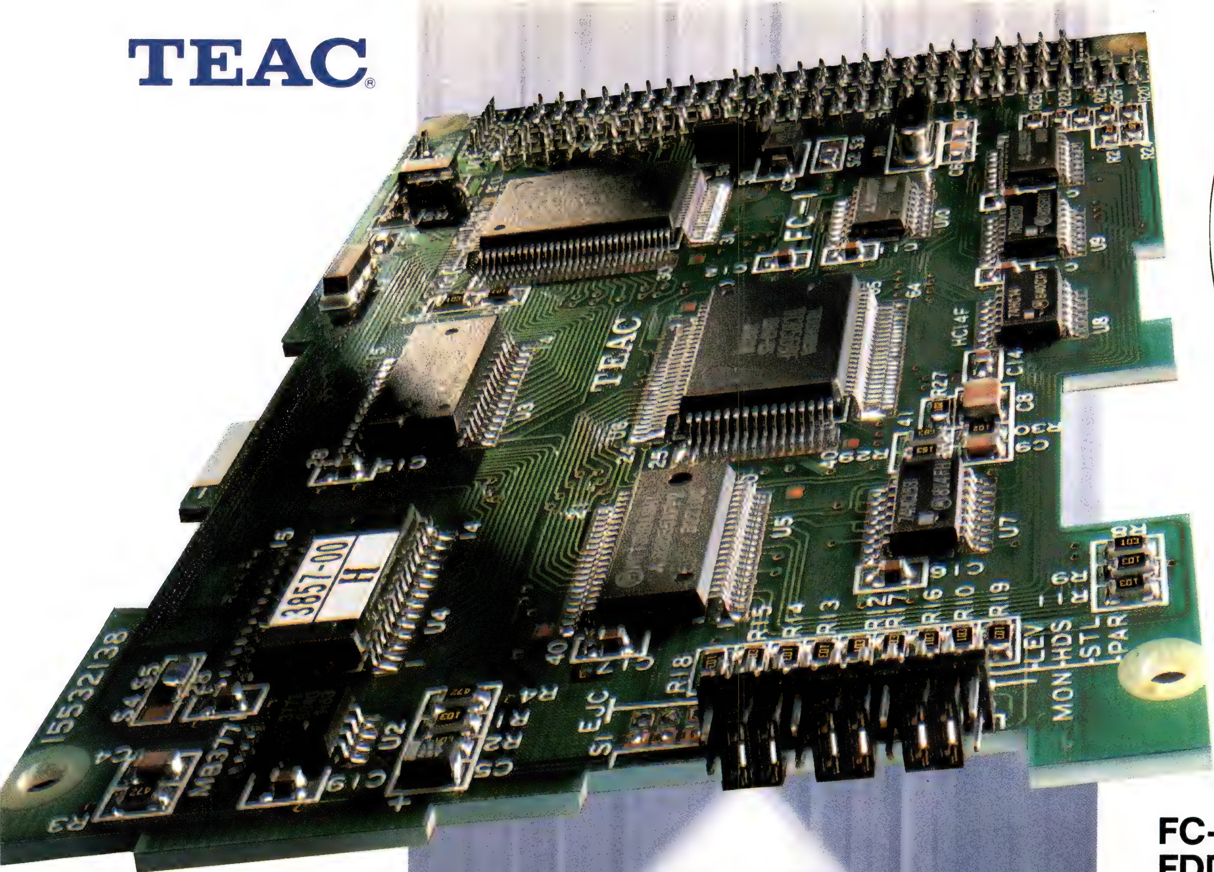

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OPTICAL-CHARACTER-RECOGNITION SOFTWARE

Inexpensive software reads printed material

Powerful personal computers run software that transforms a raw bit map, derived from an optical scan of a page of printed text, into an ASCII file.

Charles H Small,
Senior Editor

In the aftermath of the computer revolution it's clear that touch typists—not the meek—shall inherit the Earth. If you're one of the unfortunate hunt-and-peckers who find that keying in text or data is a burdensome chore, take heart. You can now let your personal computer do this onerous job for you. Recently introduced, inexpensive software packages can transform the output of high-resolution optical scanners into an ASCII file.

Optical-character recognition (OCR) offers the promise of painless, completely accurate data entry from printed material directly into your computer. Despite all the nifty things that imaginative people suggest you *could* do with your personal computer, EDN's research reveals that engineers devote a major portion of their personal computer time to plain old word processing and spreadsheets.

Engineers find themselves having to enter bits and pieces of text and data into their word processors and spreadsheets from a variety of sources. These sources include spec sheets, price lists, printouts from mainframe computers, official and voluntary standards documents, as well as reports from manufacturing, quality assurance, and field service. This list isn't exhaustive. No doubt each engineer could think of many more such sources.

Heretofore, OCR equipment was both expensive and not particularly useful. Early OCR equipment couldn't read just any printed material; you had to prepare your copy on special paper and use a special IBM Selectric typewriter ball. Even the slightest smudge or mistrike could confuse the computer. Later, special, computer-readable character sets (or fonts) came along—the most recognizable being the MR11 (**Fig 1**).

Such fonts are still very much with us. And you can get hand-held scanners with which to read them from makers such as Caere Corp. You can design these handheld scanners into applications where you might alternatively use a bar-code a magnetic-strip reader.

Although high-resolution scanning hardware has been available for some time, low-cost OCR systems that can read an entire page have not. That's be-

The OmniScan omnifont OCR software *from Caere Corp can translate the output of handheld scanners as well as conventional page scanners.*

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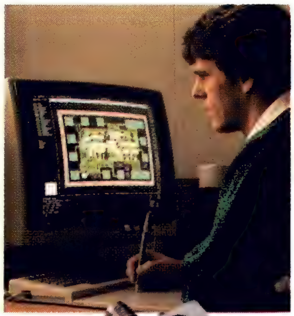


AVANTEK

Optical-character-recognition software

cause the real trick to reading fonts not expressly designed for computer input is lots of processing power and memory capacity in the computer, which mulls over the scanner's output.

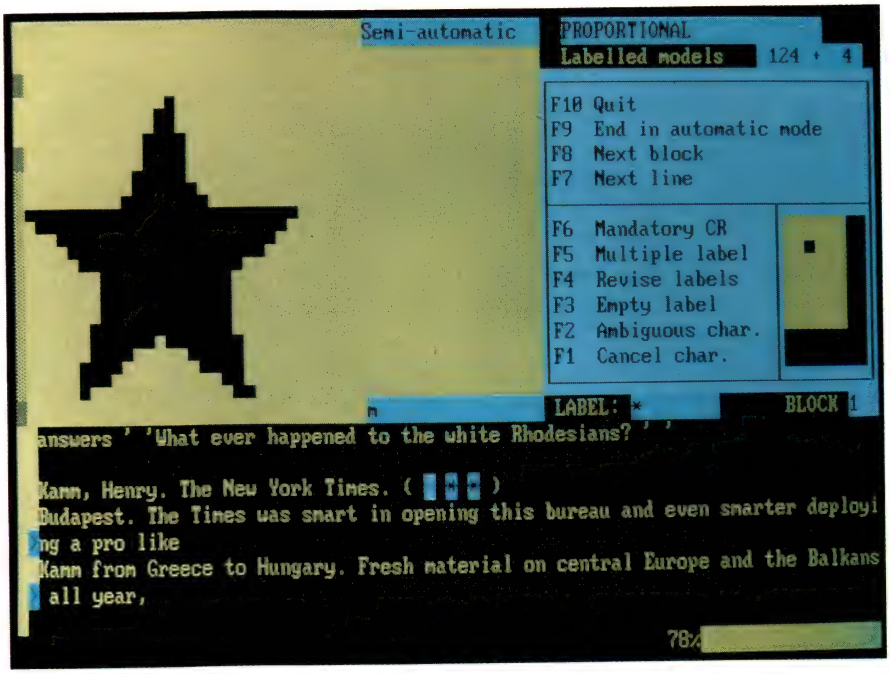
Reading isn't easy

Consider the magnitude of the task the computer faces. First, a high-resolution, 300-dpi scanner will produce a 1M- to 2M-byte data file from a single 8×11-in. page.

Also consider that the conservative estimate of the number of commonly encountered fonts is 2000. And, if the sheer number of different fonts isn't enough of a problem, typesetters have their own little tricks that further complicate the OCR software's job. In addition to proportional spacing, typesetters execute a process called kerning to slightly squeeze or expand the letters on a given line to make a column's margins exactly even. Thus, on a given page, even if the page's printing uses only one font, not all of the letters on the page will be exactly the same shape.

But if you look closely at printed material, such as the copy of EDN you're reading now, you will become aware that typesetters and magazine designers use a variety of fonts and character sizes on a given page to dress it up. And, while typewritten material generally has only one large column per page, typeset material often has multiple columns that snake hither and yon around the page. We've all had the experience of getting lost while trying to follow the column breaks around a badly layed-out page. OCR software can find such pages equally confusing.

To be useful to engineers, OCR software also has to be able to read tabular material. And with the advent of the laser printer and desktop-publishing systems, typewritten documents having nothing but simple, consistent letters and no line drawings, tables, or photos are fast disappearing. Virtually anyone can now produce documents that have a variety of typefaces and type sizes, along with a rich variety of tables and artwork.



The ReadStar Express OCR program *combines omnifont scanning with optional training sessions to allow the program to recognize special characters.*

Additionally, OCR software has

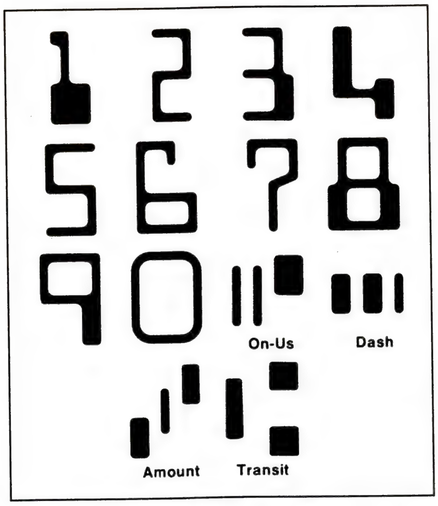


Fig 1—Computers have an easy time *reading specially designed characters such as these. Recognizing printed characters such as those used in this magazine is much harder to do.*

to contend with a lot of artifacts on the page that are *not* text. Magazine pages and spec sheets have photographs and line drawings; they also have other embellishments and decorations (called dingbats, believe it or not). Depending on a font's design, OCR software can have trouble separating letters because between 10 and 50% of the letters in a given font can be joined. What's more, the ASCII character set has far fewer total characters available than do fonts for typeset material. For example, typeset material uses different characters for opening and closing quotes where the ASCII character set has only one quote character. Typeset material uses different characters for minus signs, dashes, and hyphens where, again, ASCII has only one.

You should not be surprised to learn that effective, low-cost OCR software awaited the arrival of the more powerful versions of the IBM PC and the Macintosh.

Right now, inexpensive OCR software for personal computers

breaks down into two basic categories: "omnifont" software, which automatically recognizes any font, and "trainable" software, which you must train to recognize each new font as the software encounters it.

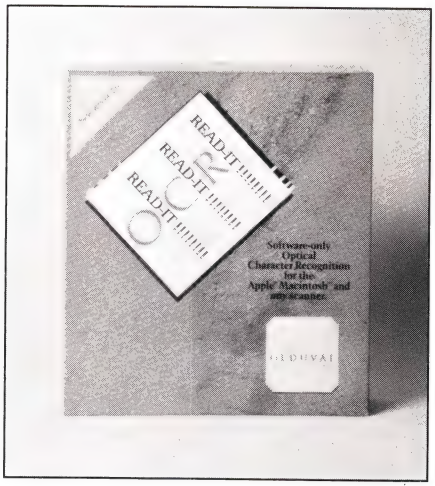
Historically, OCR software progressed from programs that recognized only a few, preprogrammed, computer-readable fonts, to trainable programs with which you could develop a library of fonts that the software could read. Using a trainable OCR program, you need to spend 5 to 15 minutes going over a page or two of text interactively before the program will be able to read the new font reliably. Consequently, trainable OCR programs prove bothersome for some short documents or uncommon fonts. To make OCR programs useful for even a single page and to reduce the headaches associated with managing a library of fonts, vendors developed omnifont OCR software.

Companies keep secrets

The inner workings of OCR software would probably be fascinating to learn about—if only the vendors would reveal them. Alas, they regard their algorithms as proprietary company secrets and will not discuss them in public.

According to one OCR-software maker, Inovatic, first-generation OCR software uses matrix-matching techniques to recognize characters. First-generation OCR software compares the bit map of a character, pixel by pixel, with a table of pre-defined matrices, looking for a match. Because two scans of the same image rarely yield identical bit maps, matrix-matching OCR software must have a relatively high tolerance for near matches. After all, the files comprise millons of bits.

This requirement results in a degradation of accuracy as the fine information required to discriminate between innately similar characters such as a "b" and a "6" often gets lost within wide tolerance limits. The associated matrices of the more complex fonts must perforce become more complicated; therefore both recognition speed and accuracy tend to fall when these fonts are used.



***The Read-It! OCR software from** Olduvai Corp comes with many common fonts already entered into its libraries.*

The next step for OCR software was the development of feature-extraction methods. Feature-extraction software uses a set of rules about characters based on the characters' appearance. A character comprising an arc attached to the top and mid-point of a vertical line, for example, could be a "p" or a "P."

The task of finding unique descriptions for all characters and then translating the descriptions into terms a computer can understand can be monumental. Try, for example, to describe the difference between "5" and "S" while keeping in mind that your description must apply to a wide variety of fonts. And consider that concepts such as "straight" and "vertical" can often be ambiguous when dealing with 300-dpi representations of pages that are not always laid perfectly squarely on the scanner.

Your instruction must also be able to distinguish between serifs (the decorative flourishes found on the endpoints of many characters), and truly distinguishing features. Handling all possible exceptions often results in a large feature-extraction rule base, which in turn consumes more memory than most PCs have.

Inovatic claims to use proprietary "elastic" mathematical models in its "third-generation" OCR software, which it considers to be a better

***The Datacopy AccuText OCR program recognizes indents,** tabs, margins, returns, and other page-formatting commands. The Xerox Imaging Systems' program inserts the appropriate codes for these page-formatting commands into the ASCII file it passes on to the computer's word-processing program.*

Optical-character-recognition software

method of character extraction.

Presently, four vendors have low-cost OCR software. The software packages differ in two ways: some are omnifont while some are trainable, and some require an add-in board while some do not. Most claim to be able to digest the output of virtually all commercially available, high-resolution scanners.

Caere Corp claims its OmniScan omnifont OCR software can translate 40 to 115 cps from a consistent font. The characters being read can range in size from 8 to 72 points (one point≈1/72 in.). In addition to automatically recognizing any font, OmniScan can separate drawings from text and read tabular material. You can also set it up to ignore certain portions of a page and to follow column breaks.

The software can accept files from fax modems; it produces files compatible with Lotus 1-2-3, Microsoft Excell, and Ashton-Tate dBASE, as well as files for most common word processors.

OmniScan requires an IBM PC with 640k bytes of RAM, a hard disk, and MS-DOS 3.1 or later. It requires a mouse and runs under Microsoft's Windows 2.0 or later. The package for 80286-based PCs comes with a Motorola 68020-based add-in board, which has 2M bytes of RAM. The version for 80386-based PCs requires no add-in board and runs under either MS-DOS or OS/2.

Recently announced add-ons for OmniScan claim to enhance its accuracy and expand its usefulness. OmniSpell is a $99 spell checker that goes over the output of OmniScan looking for spelling errors. OmniSpell has dictionaries for 10 popular Indo-European languages and Finnish.

OmniDraft also costs $99 and can make sense of the otherwise hard-to-scan output from dot-matrix, draft-quality printers. OmniTrace costs $150 and it converts bit-mapped artwork into PostScript-compatible artwork files. With OmniTrace, you can scan both text and drawings and submit the converted files to the PostScript desktop-publishing program.

Caere offers package deals that include software, an add-in board (as needed), and a Cannon scanner. Prices for 80206 PCs range from $3185 to $4380, depending on the scanner selected, and $2085 to $3280 for 80386 PCs.

Inovatic, on the other hand, does not package scanners with its Read-

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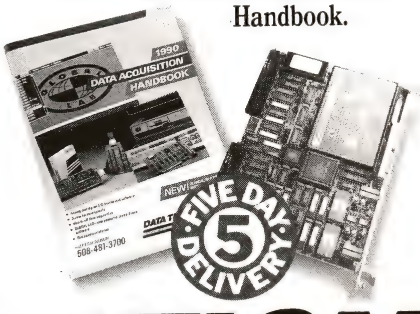

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DT1492-F	8DI	12	1, 2, 4, 8	150	2	130/DAC	16
DT1492-G	16SE	12	1, 2, 4, 8	250	2	130/DAC	16
DT1492-G	8DI	12	1, 2, 4, 8	250	2	130/DAC	16
DT1492-L	4DI	12	1	750	2	130/DAC	16
DT1495	16SE/8DI	12	1, 10, 100, 500	40/2.5	2	130/DAC	16
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Optical-character-recognition software

Star Express omnifont OCR software. Nor does it require an add-in board. The $995 program, unlike other OCR software, first compresses the scanner's output down from a megabyte-range file into a hundred or so "signs"—to use the term fashionable among semioticians.

As a result of this compression, ReadStar Express can run on 80286-based PCs without an add-in processor board because the compressed page file does not overwhelm such PCs' 640k-byte memories. Inovatic does not quote a character-conversion rate for its program.

The program automatically differentiates between text, graphics, headlines, and multiple columns. It can also recognize tables and automatically suppress images and logos. One minor detail: You can supplement the program's automatic analysis of a page with a manual training session.

Olduvai Corp has two versions of its Read-It! OCR software: a $195 version for hand scanners and a $495 version for page scanners. The trainable software runs on both IBM PCs and Macintoshes. The IBM edition runs under Microsoft's Windows Graphical User Interface (GUI).

The programs come with many common fonts already entered into libraries. It takes about 15 minutes for you to train the programs to recognize another font, the company claims. The programs can handle from 6- to 48-point type. The hand-held-scanner version doesn't just recognize special, computer-readable fonts; you can use it, in conjunction with a hand-held scanner, to enter text and data from virtually any source. You can also set it up to read tables.

The software can read standard files from many common hand-held scanners, including the Logitech ScanMan, DFI, and The Complete PC scanner. It also works with page scanners such as those from Canon/Princeton, Microtek, and Hewlett-Packard' Scanjet. The text files it produces are compatible with most word processors, database programs, spreadsheets, and desktop-publishing systems. The program will run on an 80286-based IBM PC without an add-in processor board.

Datacopy AccuText software from Xerox Imaging Systems (formed by a merger of Datacopy and Kurzweil Computer Products), purportedly brings artificial-intelli-

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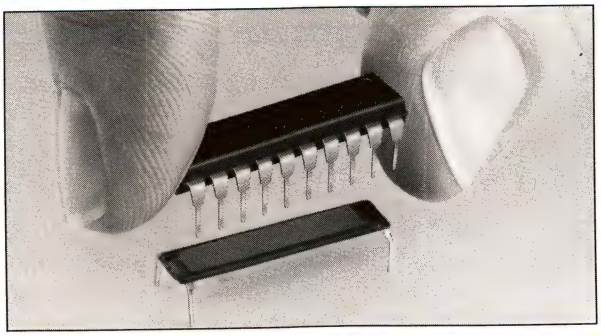

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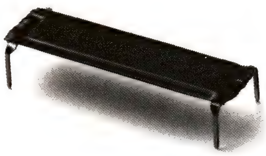

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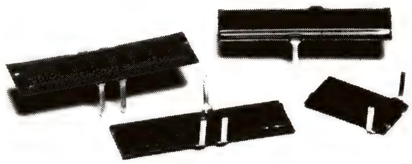

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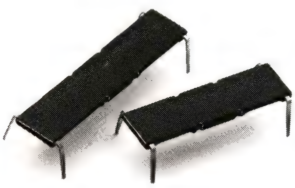

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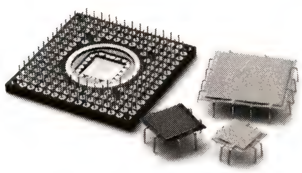

CIRCLE NO. 111

Optical-character-recognition software

gence techniques to bear on the task of reading text. The $995 program runs with a 68020 accelerator card on either the Macintosh II or the Macintosh SE and requires 4M bytes of system memory.

The program handles the output of most scanners including the company's various JetRead models, the Apple Scanner, and HP Scanjets. It can translate 6- to 24-point type. In addition to text, the software develops a range of formatting information, "hard" carriage returns, bulleted lists, and tabs for material organized in columns.

AccuText can capture line-art images, along with printed text, and generate user-specified half-tone images in standard image-output formats such as the one used for MacPaint. You can vary the resolution of artwork from 75 to 400 lpi.

The program also has a 50,000-entry dictionary. It employs usage information in the dictionary to resolve ambiguous translations at the word level based on the word's context. Most other OCR software simply tries to recognize each letter individually. The firm offers programs with context-sensitive dictionaries for English, Spanish, Italian, German, Dutch, Swedish, Norwegian, and French. You can add up to 10,000 words of your own to the program's dictionary. Revealingly, the program is so automatic that it has no provision for user training.

Scanner cost is high

Although low-cost OCR software is now available, high-resolution optical scanners are still rather expensive. Perhaps hardware designers will be inspired to re-design high-resolution scanners to bring their prices down in line with the software's. What's more likely is that scanner prices will remain expensive while their performance will increase. Scanners' resolution will increase from 300 to 400 dpi or even 600 dpi, grey-scale resolutions will increase from 4 to 8 bits or 16 bits, and color scanners may even appear soon. EDN

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

For more information . . .

For more information on the OCR software discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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CASE FOR EMBEDDED SYSTEMS

New software tools speed design and debug

Four recently introduced CASE packages may help speed design, debug, and integration chores for your embedded system.

Margery Conner,
Regional Editor

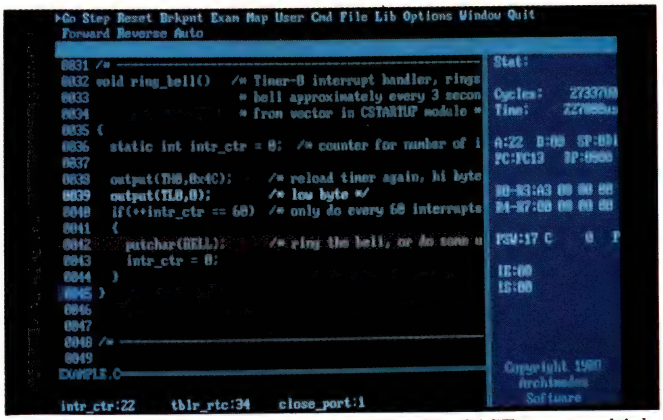
Embedded-systems design requires a delicate hardware-software balancing act. The two must be designed to complement each other. If you spend too much effort in the design of one before checking it against the other, you'll face extensive redesign chores. Although excellent CAE tools exist to aid hardware design and simulation, similar tools for software design and integration have lagged. In the past six months, however, four vendors have introduced computer-aided-software- engineering (CASE) tools specifically for embedded systems software design and integration.

CASE tools have been around for a long time for batch-processing systems. Most of these tools, however, are for the code-design step, and are tools for documenting code design using a structured-design methodology. Projects that use these CASE tools tend to have large teams of programmers who write millions of lines of code. Typical applications are in banking or the military.

Many of these structured-analysis packages address embedded systems by including extensions for real-time programming. The Yourdon-DeMarco method, for example, is one of the most popular structured-analysis methodologies, and the Hatley real-time extensions are the conventions used for indicating how a software module reacts to a real-time interrupt. Indeed, the prevalence of these tools labeled as "CASE" has made CASE synonymous with structured analysis. However, for many reasons, few embedded-systems designers use structured analysis. First, most embedded-systems designers view structured analysis as a method to coordinate and document a project among many engineers. Also, relatively few engineers, perhaps 15%, are familiar with a structured-analysis methodology.

In addition, there's much more to embedded-systems software than code design (**Fig 1**). Unlike traditional CASE tools for batch-processing systems, the embedded-system tools introduced recently by Mentor, Ready Systems, Archimedes Software, and Integrated Systems Inc (ISI) concentrate on the steps that follow code design: code writing, debug, integration, and performance evaluation.

The four packages, which are listed in **Table 1**, are aimed at fairly specific



Running on an IBM PC or compatible*, SimCASE uses multiple windows to provide information about its simulation of an 8051 µC running your C code.*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CASE for embedded systems

kinds of embedded systems, so you'll need to know which package best suits your application. For example, Mentor's Codelink Station is aimed at simpler systems operating without a kernel; Ready Systems' CARDtools is aimed at systems operating under the company's real-time kernel. Archimedes' SimCASE supports only systems running on an 8051 μC (microcontroller); Integrated Systems Inc's Matrix tools can handle most general kinds of systems.

Codelink does not assume that you have used a structured-analysis methodology for your code design. As long as your C code complies with IEEE-695A, Codelink's Structure Recovery portion reverse engineers your code to create a structure chart. This structure chart serves as a graphical road map of your software that you use to select any portion of the code. Once you've selected the code, you can examine, modify, or run it on simulated hardware. In Codelink's virtual mode, ISS (Instruction Set Simulator) generates object code from the source code you write. The object code then serves as the stimulus to the company's hardware simulator, QuickSim, which flags any logic errors. QuickSim runs in batch mode using the ISS-derived signal as the input stimulus to a bus-functional hardware model.

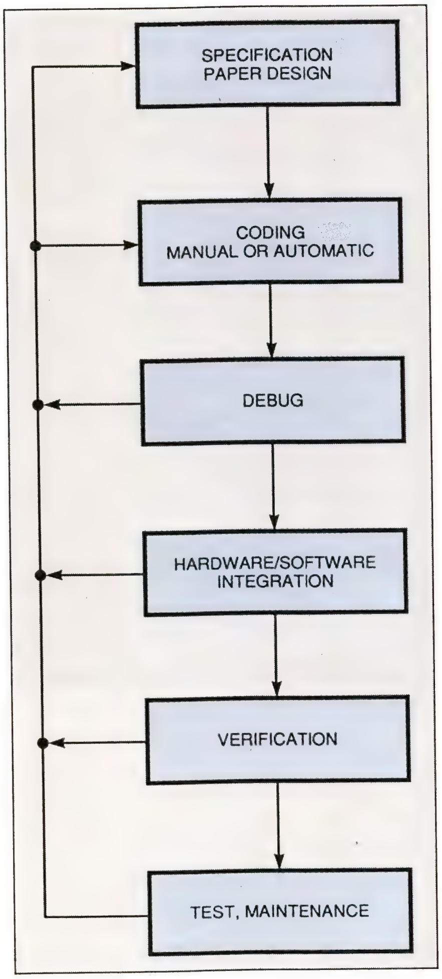


Fig 1—Embedded-systems software design tools differ from traditional CASE tools *for batch-processing systems in that they concentrate on the steps that follow code design.*

De facto division of labor

Be aware that timing conflicts are not automatically flagged; rather, they must be caught by the astute hardware designer. According to Rick Potter, general manager of Mentor's CASE division, there is a wall between software and hardware development in most embedded-systems designs. Usually, the software engineer writes code independently of the hardware designer. He added that the most likely scenario for coding is where the programmer hands the code off to the hardware designer, who will supervise the integration of hardware and software.

Thus, you cannot specify the software's behavior at the system level. The hardware simulator only tells you that it didn't get the expected output for a given input vector; it doesn't give you any analysis as to why you didn't get the correct output vector.

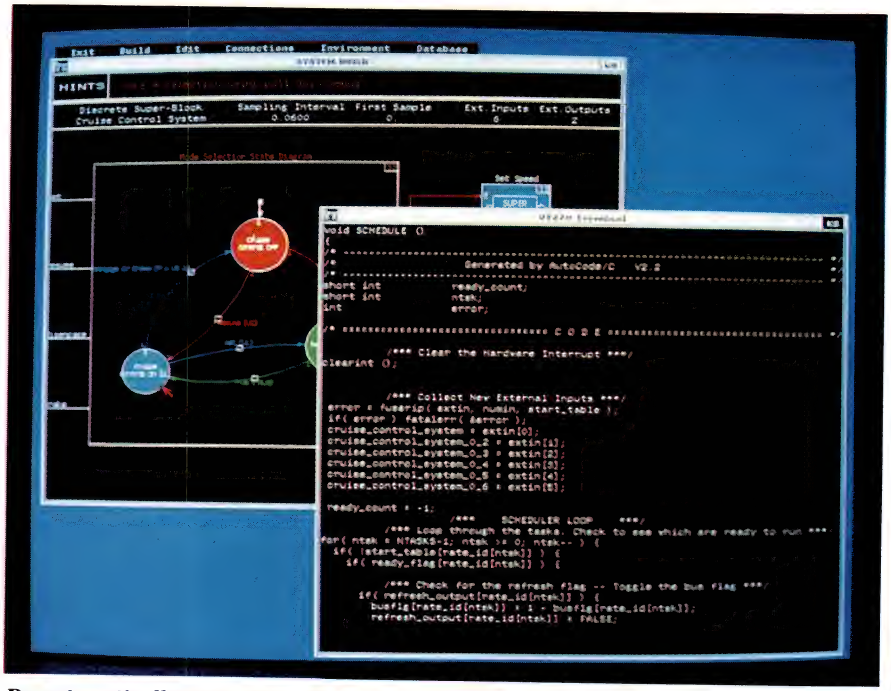
Also, be aware that if you should change the code, the structure chart is no longer any good. You

Table 1—Representative CASE tools for embedded systems

Vendor/Tool	Real-time operating-system support	μP	Workstation	Languages	Price	Comments
Archimedes Software SimCASE	Intel	8051	PC/AT	C	\$995	SimCASE is an 8051 simulator.
Integrated Systems matrix	All	μP independent	Sun, DEC, Apollo, PC/AT, PS/2	C, Fortran, Ada	\$20,000-120,000	Matrix is an analysis, design, modeling, code generation and simulation package.
Mentor Graphics Codelink station	None	All	Apollo	C (IEEE-695A)	From \$27,900	Codelink performs behavioral and timing analysis through Mentor's QuickSIM hardware simulator. It also links to Hewlett-Packard's 64700-series emulators.
Ready Systems CARDtools	VRTX	680X0, 80X86, 29000	Sun 3, VAX mainframes and VAX-stations	Not language dependent	From \$7000	CARDtools TaskTimer combines user estimates of application module and hardware timing with its calculations of VRTX timing requirements to generate a system timing simulation.

must rerun the structure-recovery software to have a valid chart. There is neither back annotation nor automatic checks to make sure that you indeed do rerun the structure recovery software.

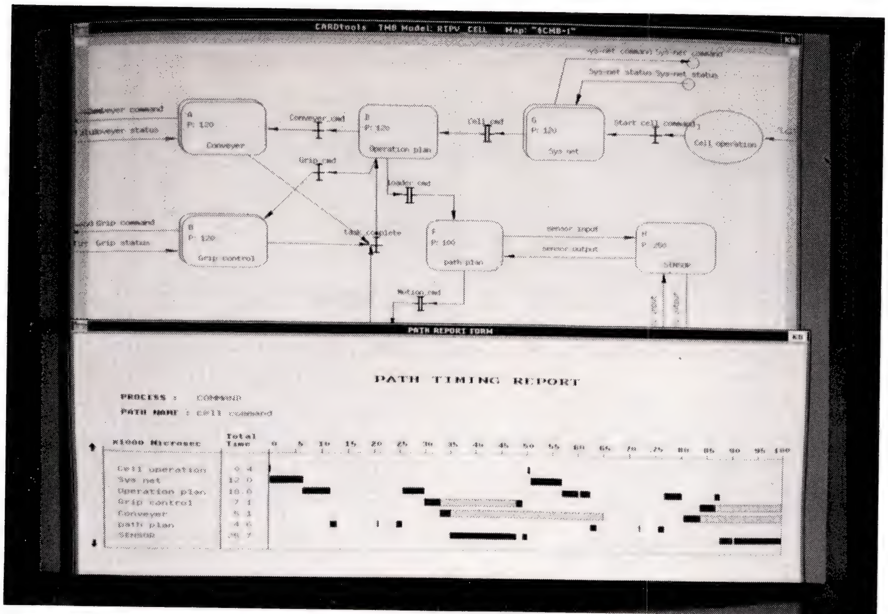
Codelink supports embedded systems that do not require an operating-system kernel. Ready Systems' CARDtools, on the other hand, supports complex multitasking systems that use the company's VRTX real-time operating system. And unlike Mentor's approach, which assumes that the ultimate responsibility for system integration is the hardware designer's, CARDtools supports system design from a software designer's point of view. For example, hardware is represented in simulations as a black box, whose only characteristics you know are its timing characteristics, such as response time.



By automatically generating C code, *ISI's AutoCode lets you try several different versions of your software before selecting the final one.*

CARDtools contains TaskTimer, a system timing performance simulator. System timing depends on two factors: the application software and the operating system. TaskTimer derives the VRTX operating system's response time, but you must estimate the time each module in your application software will take to run.

Thus, TaskTimer's simulation is only as good as your timing estimates for your application software and your hardware black boxes. But, by forcing you to perform a timing analysis at the very beginning of your design cycle, TaskTimer can point out ambiguities and potential trouble spots before any code is written or hardware designed. Also, as you refine the estimates, you can play a "what-if" analysis and evaluate your hardware.



By displaying system timing results *in a Gantt chart, TaskTimer lets you consider multiple paths, priorities, and shared resources in your embedded system.*

Software tradeoffs

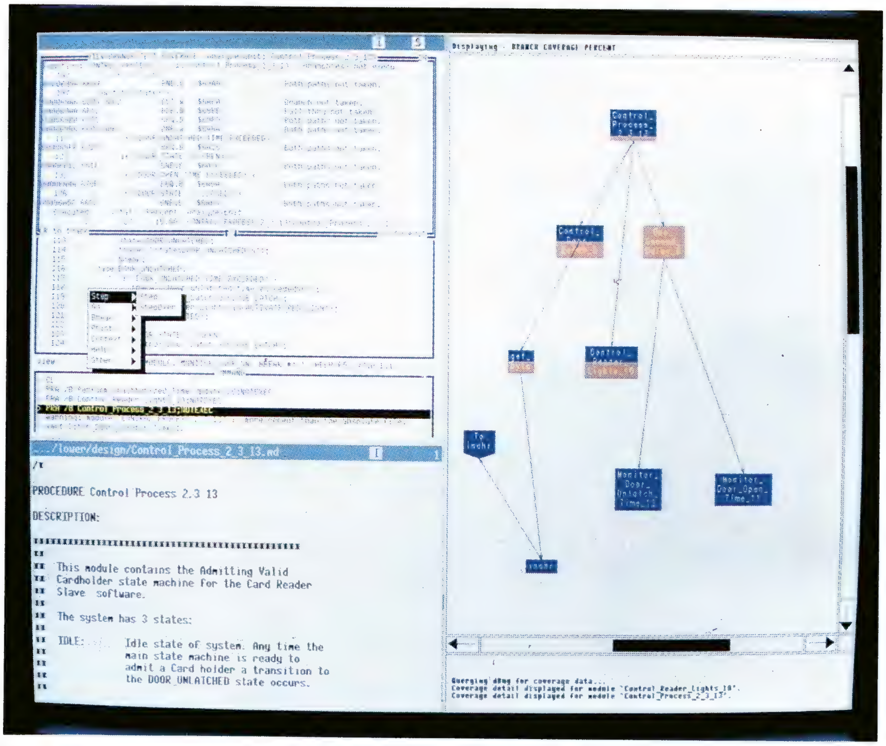
TaskTimer includes the pertinent specifications of target processors, such as cycle times or any required RAM or ROM wait states. By including these hardware parameters in a system-timing simulation, TaskTimer lets you evaluate your options in processor hardware. For example, you can check if a 68010 is fast enough. If not, you may be able to raise the system speed by using a 20-MHz version, rather than a 68020. Keep in mind that TaskTimer is concerned only with processor timing that affects how fast VRTX runs, so it doesn't need to know about other system proces-

sors, such as a dedicated DMA controller. Note too that in the design phase you can assume multiple processors, but in simulation, only one.

Along with its knowledge of the processor speeds, TaskTimer also can apply knowledge of external devices and their drivers. You can either define the external devices as drivers with a specified delay, which are completely opaque to VRTX, or you can define the devices as being under the control of VRTX. When these type of drivers run, VRTX essentially goes to sleep as long as the device is active. Nothing else can occur in parallel as far as VRTX is concerned. By involving VRTX, the operating system is able to let something else run in parallel with the device's activity.

CARDtools doesn't have the degree of accuracy that Codelink offers, but you can use it on much more complex multitasking systems. It also allows you to easily change software and hardware timing characteristics while you're still in the planning stage. An advantage to this flexibility is that you can closely examine your design partitioning—which tasks are done in hardware, and which in software.

You probably won't find this flexibility in most structured-analysis design packages, because structured-analysis methodologies are usually in the form of data-flow diagrams, which are concerned only with input. That is, through some transformation, the input becomes output. Real-time systems are concerned with the transformation itself because the time the transformation takes is critical. And the timing of the transformation will affect the software design. By estimating software and hardware module timing very early in your design, you can determine which



By converting your C source code to object code, *Codelink allows you to check your software on Mentor's QuickSim hardware simulator before you build any hardware.*

hardware and software constructs will be likely to meet your overall specifications.

Most of the focus in new CASE products for embedded systems is for the 32-bit processors and controllers. Yet the vast majority of embedded controllers are 8-bit. Archimedes Software has two CASE tools for the 8051 μC—SimCASE and SimI/O, which cost \$995 and \$695, respectively.

SimCASE is an 8051 simulator that can run your compiled C program. It also contains an input stimulus generator that allows you to synthesize any possible input to the simulated μC. The advantage of running your code through a simulator rather than through the target system via an emulator is that in a simulator you can run worst- case input conditions. For example, in most cases an input switch may debounce in 1 msec, but worst-case time is 5 msec. In the target system the worst- case condition may never occur, but you can force the condition with a simulator. You'll need SimI/O to simulate all input and output responses at the 8051's I/O ports.

You can use SimCASE with one of the real-time kernels supplied by Intel for the 8051, but Archimedes Software anticipates that most of the work done with 8-bit systems won't require a kernel.

Automatic code generation

ISI's embedded systems CASE tool set, Matrix, includes a code generator. Automatic code generators are often derided for the exhaustive thoroughness their specifications require. By the time you've specified a software module to a code generator's satisfaction, you could have written the code yourself. ISI claims that because its code generation is only for narrowly defined embedded systems, the gen-

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erator can make many assumptions that simplify your code definition. According to Naren Gupta, president of ISI, most of the company's customers are system designers rather than programmers, and systems designers like to try several designs before selecting the final one. "Our users typically throw away a million lines of code before anyone else can write 10,000," she said.

The price for the package is comparatively steep: a practical implementation can cost about \$120,000, although portions of the tools are available starting from \$20,000. As you might expect, current customers are large companies in the aerospace and automotive industries. But if you need to be able to quickly generate, test, and discard different designs, then you may save many times the initial price over the life of the tools.

It's clear that CASE tools for embedded systems will give them more capability. Perhaps the biggest area to watch for new product introductions over the next year will be from companies like Micro-Case and Hewlett-Packard, who, unlike the companies covered in this article, closely integrate hardware emulation with the software-development tools. Development tools for the embedded systems of the future will probably integrate software- and hardware-based tools like nothing presently available.

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2. Strassberg, Dan, "ICs and tools tame tough technology," *EDN*, Oct 26, 1989, pg 73.

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For more information . . .

For more information on the embedded systems CASE tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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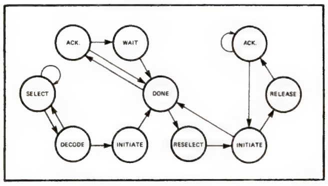

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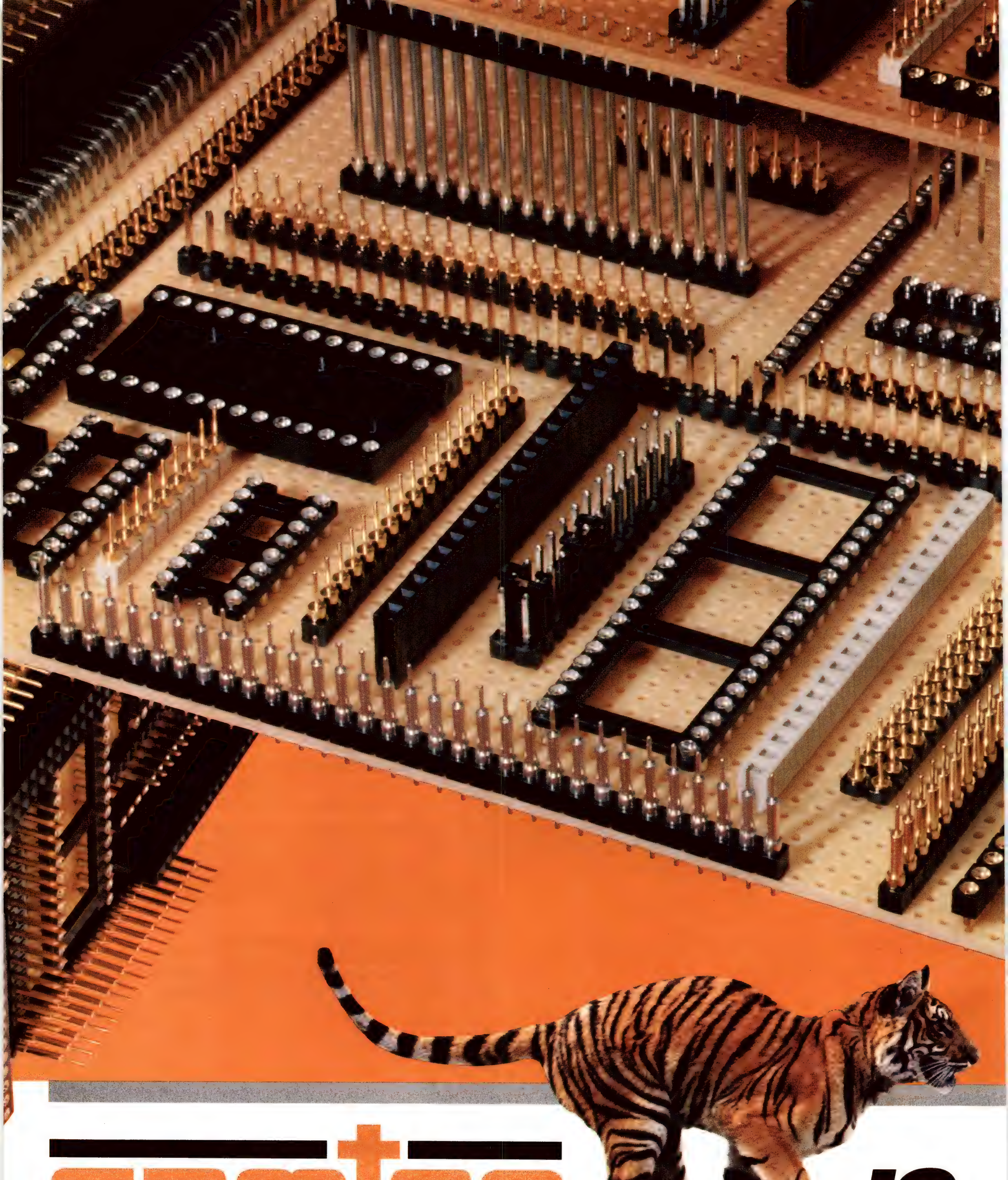
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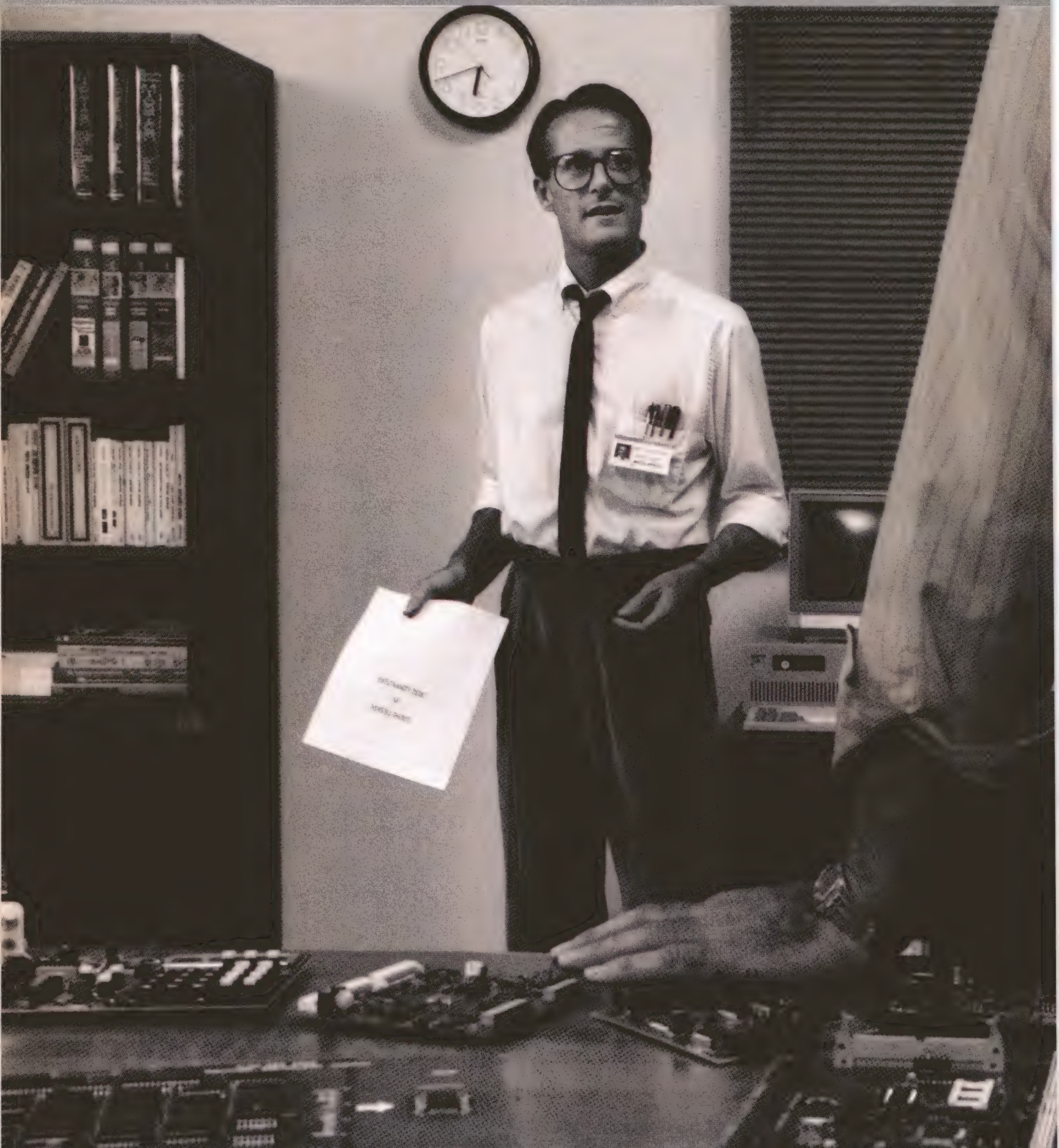

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8K x 9	72K	15	20	25		Now
4K x 18 x 2	144K	20	25	30		Now
8K x 18	144K	20	25	30		Now
64K x 4	256K	17	20	25	35	Now
64K x 4 (OE)	256K	17	20	25	35	Now
32K x 8	256K	17	20	25	35	Now
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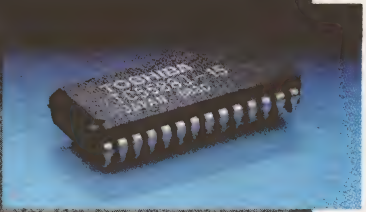

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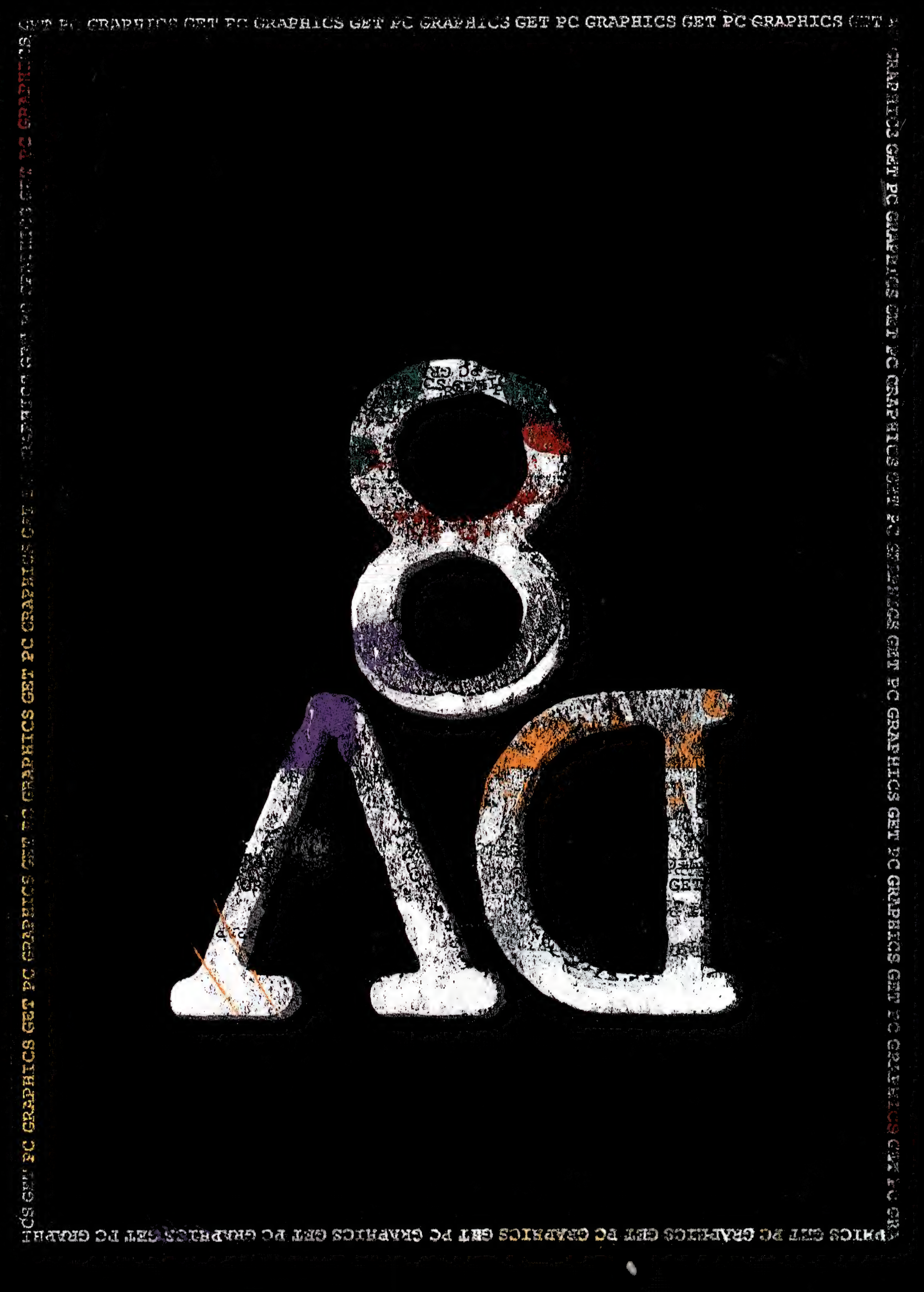
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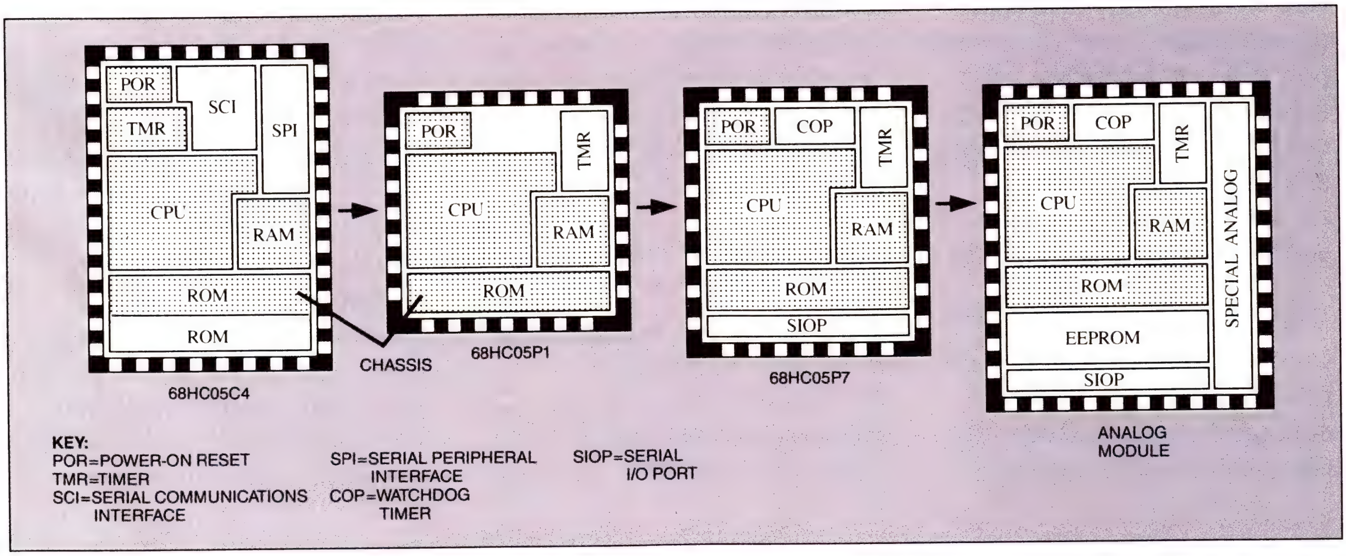

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CIRCLE NO. 71

Digital scope module extends logic analyzer

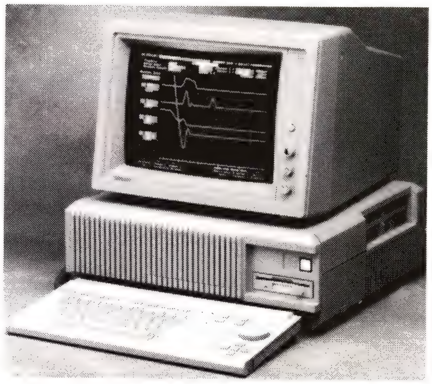
The 30DSM digital-storage-oscilloscope (DSO) module for Prism 3002 series logic analyzers isn't the first DSO to be paired with a logic analyzer. Both Hewlett-Packard (Palo Alto, CA) and Orion Instruments (Redwood City, CA) have offered DSOs combined with logic analyzers. The distinguishing features of the 30DSM are a 300-MHz bandwidth, a single-channel sample rate of 500M samples/sec (250M samples/sec dual channel), and 8-bit resolution. These specifications make it the highest performing DSO to be integrated with a logic analyzer.

One of the benefits of a combined logic analyzer and DSO is cross-triggering. The logic analyzer sends a trigger signal to the DSO when it detects a trigger event. A Prism 3002 series logic analyzer and a 30DSM combine to support a cross-triggering mode, in addition to other DSO triggering modes.

Another benefit of the combined logic analyzer and DSO is a time-correlated display of digital and analog waveforms. On the same instrument display, you can simultaneously check analog and digital waveforms and their timing relationships. This time-correlated display helps speed your operations when tracking down problems or verifying circuit operation.

Although the DSO module does not have as complete a set of automatic parameter measurements as you would find on a high-performance stand-alone DSO, it does offer frequency, time-interval, amplitude, and cursor measurements.

Some other features of the 30DSM that are useful on repetitive waveforms are its averaging function to reduce noise and its envelope mode to capture waveform variation over time.



The 30DSM is a high-performance DSO module for the Prism 3002 logic analyzer. The module provides two 300-MHz bandwidth channels having 8-bit resolution. The DSO display is time correlated with logic analyzer data.

The digital-scope module stores data in a 32k-word record for single-channel acquisitions and in two 16k-word records for dual-channel acquisitions. Nonvolatile storage of waveforms and instrument setups are possible on the Prism 3002 series platform disk.

The 30DSM rounds out the capabilities of the Prism 3002 system, whose logic-analysis capabilities include state analysis, or synchronous clocking, to 300 MHz; timing analysis to 2 GHz; and dual-threshold margin analysis to 200 MHz. The Prism 3002 also has ROM-emulation capability to speed debug operations.

The Prism 3002 series accommodates any combination of logic analysis and DSO modules to a maximum of 10 modules. The 30DSM sells for $6000.

—Doug Conner

Tektronix Inc, Logic Analyzer Div, Box 12132, Portland, OR 97212. Phone (800) 245-2036.

Circle No. 731

CIRCLE NO. 72

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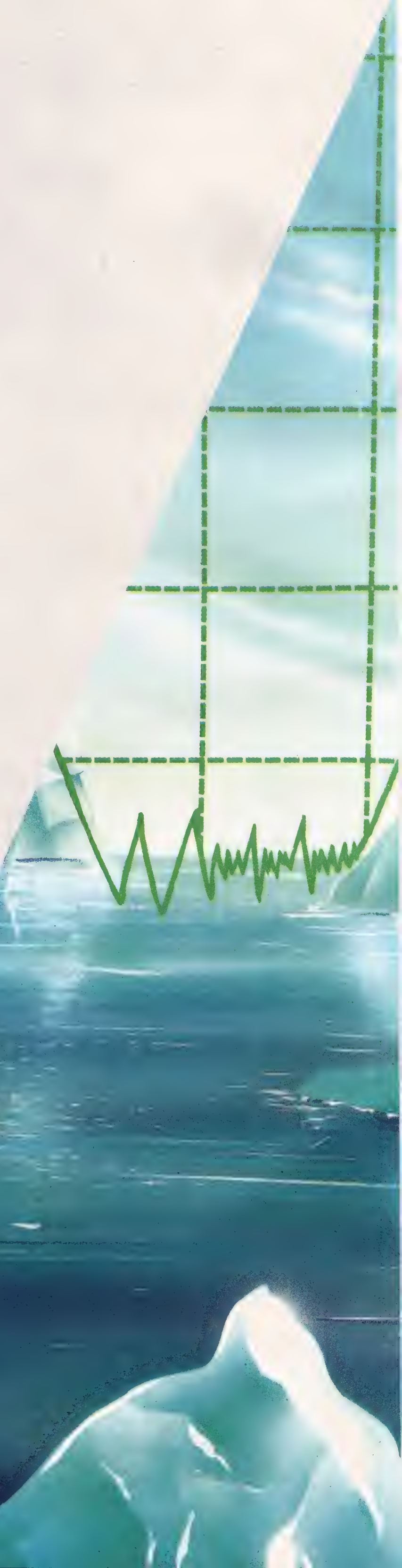

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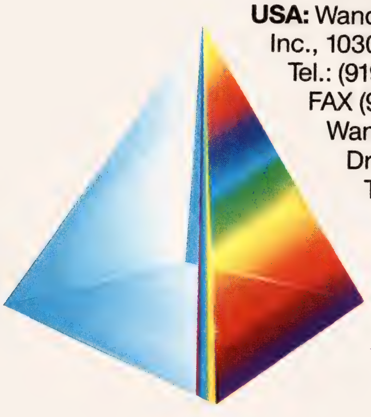

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CIRCLE NO. 131

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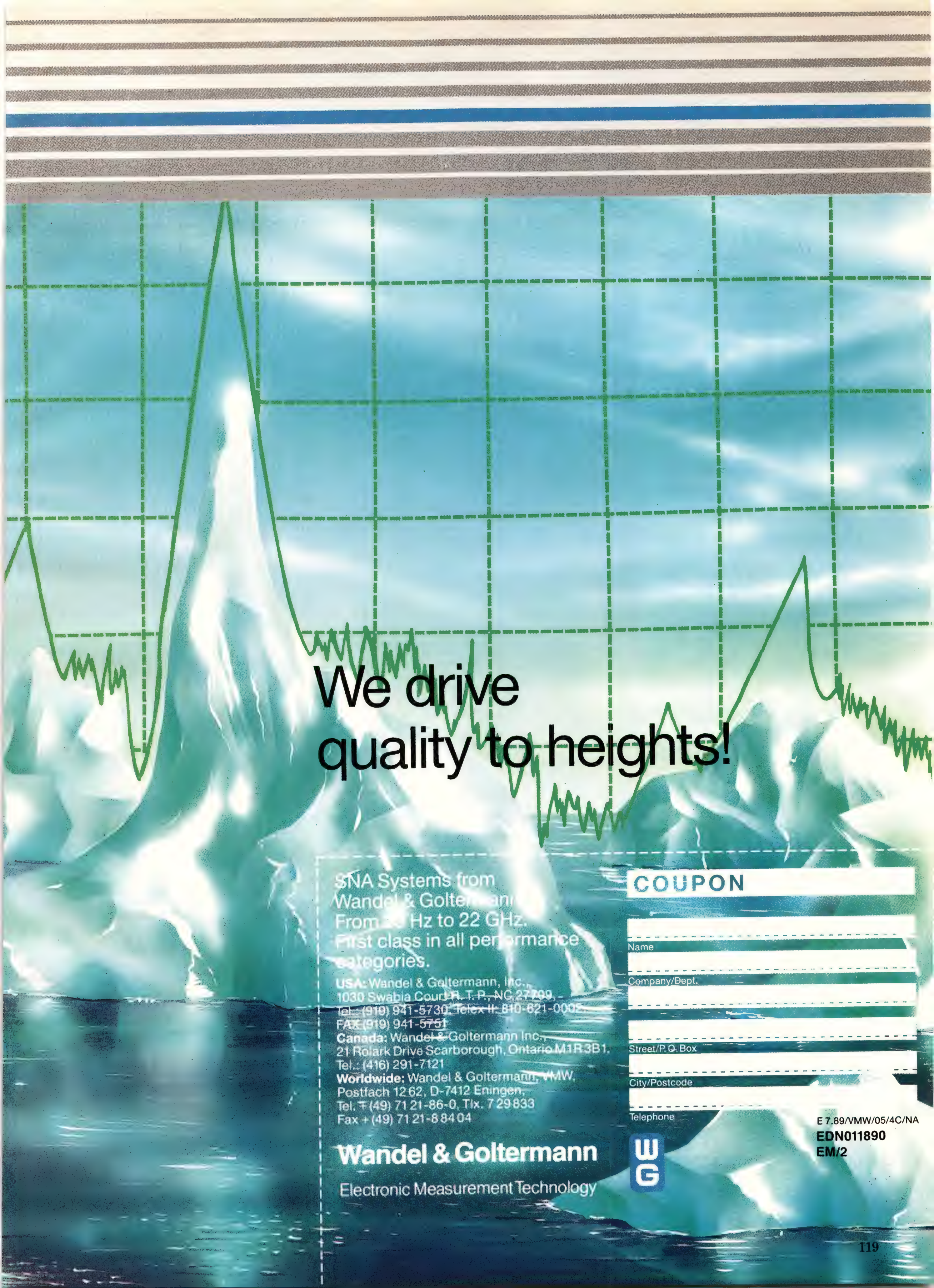

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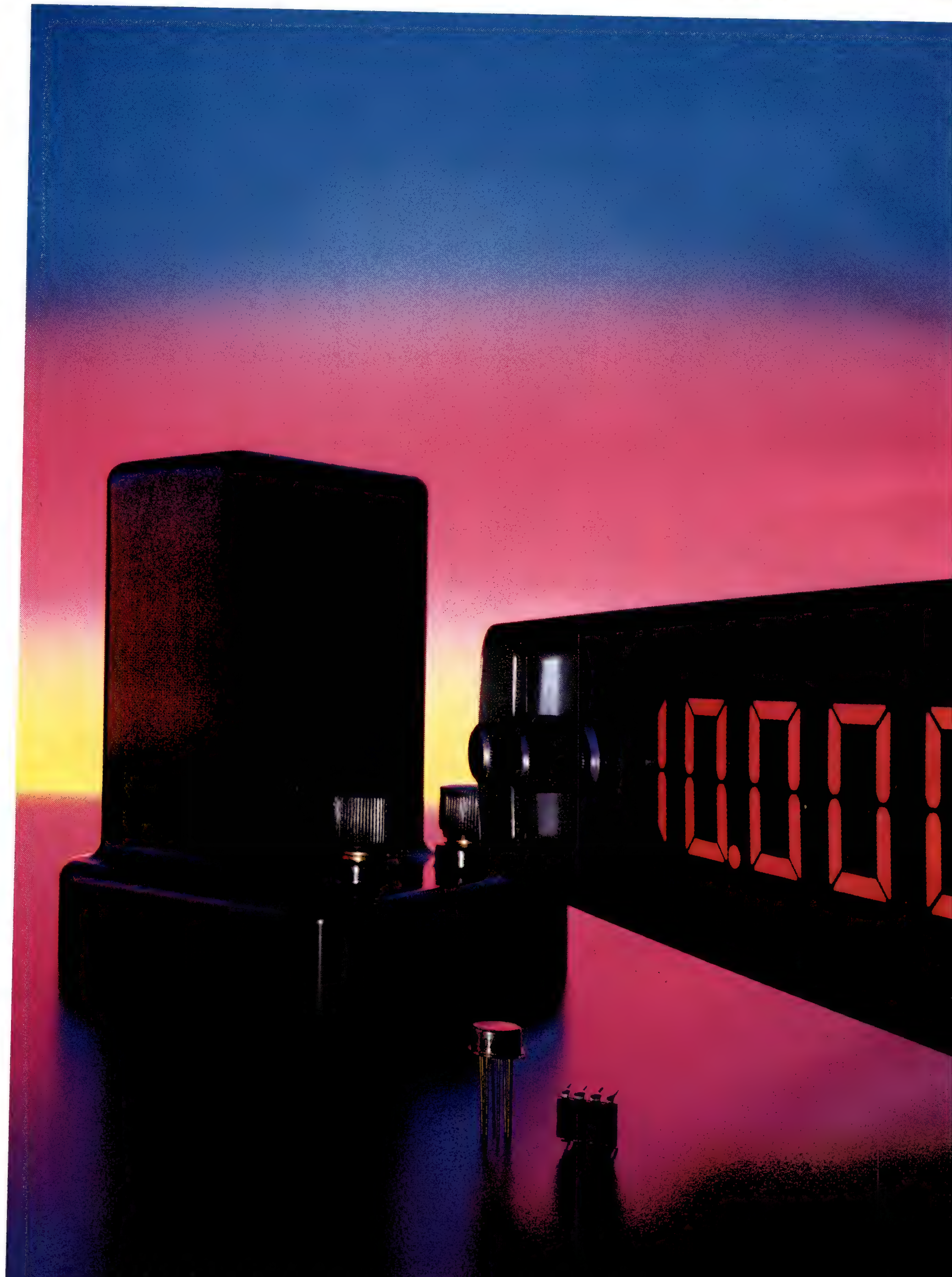
REPORT

Although seemingly mundane, voltage references play an important role in a wide range of applications. Manufacturers offer a variety of types from which to choose, but choose carefully and with an eye to what's important for your application.



Monolithic IC voltage references, *such as the REF102 from Burr-Brown, are lowering the price of long-term precision. (Photo courtesy Burr-Brown Corp; photography by Brad Hansel, Eglin Photography)*

Voltage references

Integrated-circuit voltage references are available in a variety of voltage ratings and package styles and with widely differing specifications. All, however, base their performance on the action of either a zener diode or a bandgap cell, each of which has its own peculiar set of characteristics. The most widely used reference is probably the temperature-compensated zener diode, particularly for voltages above 5V. Although bandgap cells are often scaled to provide voltages as high as 10V, the principal advantage of a bandgap reference lies in its ability to provide a stable low voltage such as 1.2, 2.5, or 5V. Before looking at the specifications of some of the available devices, consider how each of the two basic types works.

Although discrete zener diodes are available in voltage ratings as low as 1.8V to as high as 200V, they don't make very good references. The typical 10% tolerance and poor temperature characteristics of these devices preclude their use in applications requiring even a moderate degree of precision and stability. Moreover, zener diodes rated at less than about 6V suffer from high output impedance. For these reasons, discrete zener-diode-based references include temperature compensation and, in the case of IC types, the additional circuitry needed to obtain specific performance objectives.

A zener diode has two distinctly different reverse-bias characteristics: zener breakdown and avalanche breakdown, both of which are evident in the 4- to 6V range. The zener breakdown voltage **(Fig 1)** *decreases* as the temperature increases (negative TC); the avalanche breakdown voltage *increases* as the temperature increases (positive TC). At low current values, the zener effect dominates; at higher values, the avalanche effect dominates. Because these current-dependent effects oppose each other, you can, at least theoretically, cancel them by adjusting the operating point, thus obtaining a TC of zero.

Practical temperature compensation

Another way to provide temperature compensation is by connecting a conventional forward-biased diode in series with a zener diode operating in the avalanche mode. In this case, the negative TC (-2 mV/°C) of the conventional diode cancels the positive TC of the zener diode. Manufacturers use this method in most zener-based references.

If you're primarily concerned with temperature stability and the exact reference voltage is unimportant, a good combination might be a 5.6V zener diode in series with a single forward-biased diode. **Fig 2** illustrates this simple circuit. The 0.7V typically developed across forward-biased diode D_1 adds to the 5.6V of zener diode D_2 to provide a temperature-compensated reference of about 6.3V. Resistor R_1 sets the current level through the diodes. Although you can buy such a diode combination in discrete form (the 6.2V 1N821 series is

Dave Pryce,
Associate Editor

Although they are available in a wide range of voltages, the typical 10% tolerance and poor TC of a conventional zener diode preclude its use as a reference.

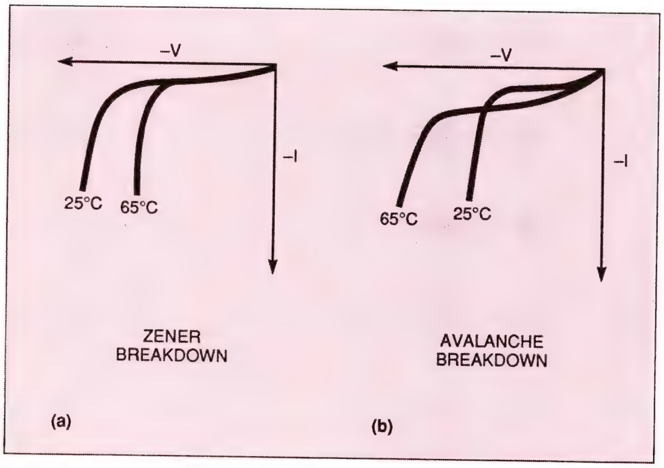


Fig 1—A zener diode has two different breakdown characteristics. *In the zener mode **(a)**, the breakdown voltage decreases with increasing temperature. In the avalanche mode **(b)**, the breakdown voltage increases with increasing temperature.*

similar), most voltage references come in IC form, which offers advantages over discrete versions.

In its most basic form, the circuit for a zener-based IC reference is similar to that of **Fig 3**. The IC can be either a hybrid or monolithic type; the choice depends on the manufacturer's objectives and processing capabilities. In this circuit, R_4 provides the startup current for the diode combination, thus setting the positive input of the op amp at V_Z. R_3 sets the desired bias current for the diode combination. The current through R_3 equals $(V_{OUT} - V_Z)/R_3$ and remains at that value, independent of the supply voltage and amplifier loading.

A zener-based IC reference has several advantages over a simple discrete reference. Manufacturers can scale the output voltage to a value different from that of the zener voltage and, by trimming the ratio of R_1 to R_2, set the output voltage to the desired accuracy. It's also possible to trim R_3 to optimize the bias current of the zener diode, thus decreasing its output temperature coefficient.

Many of today's monolithic zener-based references have ion-implanted buried zeners, which exhibit superior TC characteristics and better stability over time than do surface-based zeners. TC specifications as low as 1 ppm/°C are possible for a buried-zener reference. Compared with a bandgap reference, a zener-based reference also has less output noise because the zener voltage needs less amplification than does a 1.2V bandgap cell. Although frequency dependent, a typical 10V bandgap reference might have two to three times more noise than an equivalent zener-based reference.

Consider the bandgap reference

Bandgap references are available with output-voltage ratings of about 1.2 to 10V. The 1.2, 2.5, and 5V types can operate from lower supply voltages than can zener-based references, a distinct advantage in some applications. Although bandgap cells typically have a lower output impedance than low-voltage zeners, the additional circuitry used in both bandgap and zener-based references usually masks any difference.

Because the bandgap voltage of about 1.2V is often scaled to a higher voltage by an internal amplifier, bandgap references of 5 and 10V tend to have more

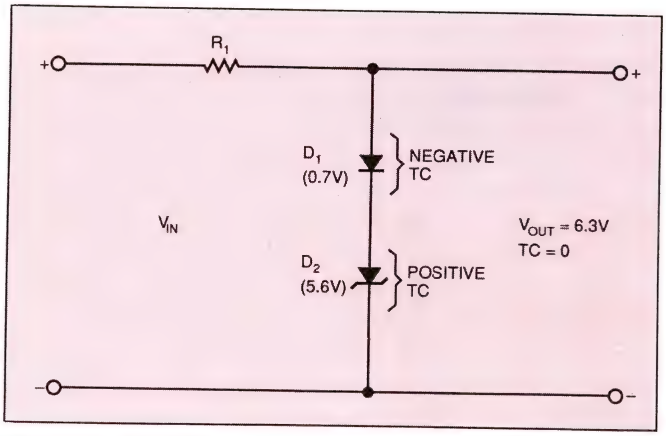


Fig 2—In this simple voltage reference, *the voltage across forward-biased diode D_1 adds to the zener voltage of D_2 to provide an output of 6.3V. The negative TC of D_1 cancels the positive TC of D_2 to provide temperature compensation.*

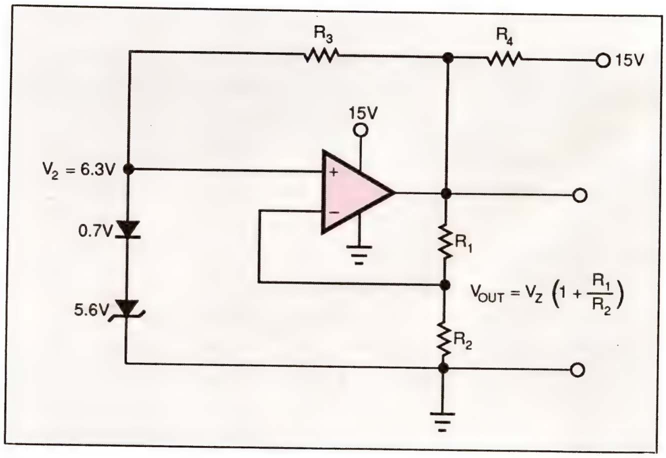


Fig 3—This basic IC reference *uses a temperature-compensated zener diode, an op amp, and voltage divider R_1 and R_2 to scale the zener voltage to a higher output voltage.*

noise than equivalent zener-based references, which need much less amplification. Moreover, the TC of a well-designed bandgap reference, although very good, is not quite as good as that of the best buried-zener references. Typically, the TCs of bandgap references range from about 5 to 50 ppm/°C.

The operation of a bandgap reference is based on the difference between the forward base-emitter voltage (V_{BE}) of two similar transistors operating at the same current but at different current densities. Extrapolated to absolute zero, V_{BE} is equal to 1.205V, the bandgap voltage of silicon. By adding a voltage to V_{BE} that increases proportionally with temperature at the same rate that V_{BE} decreases, a bandgap reference can, theoretically, generate a constant 1.205V at any temperature. Practically, however, designers can only approach that ideal.

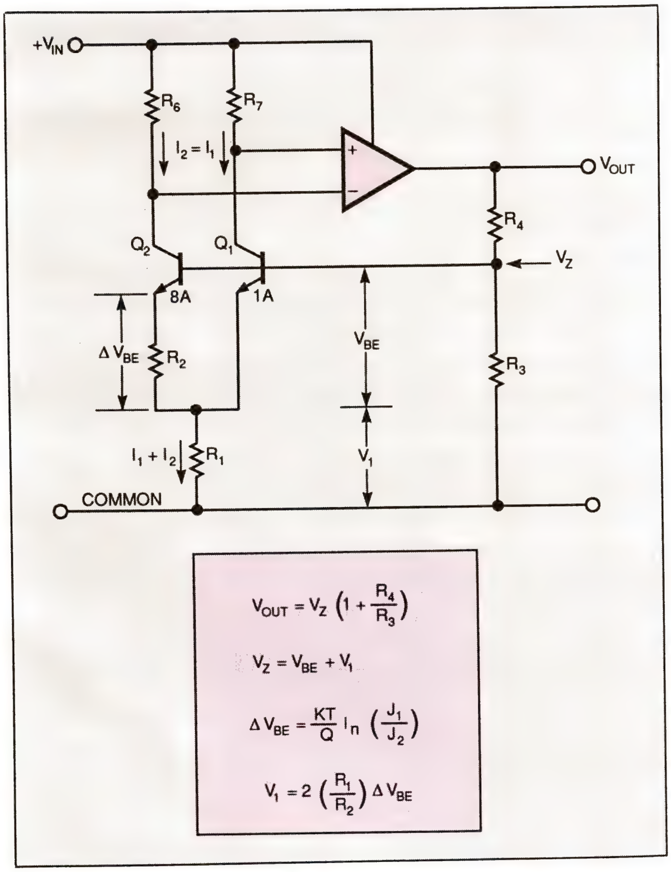


***Fig 4—The operation of bandgap reference** depends on the difference between the base-emitter voltage of two similar transistors operating at different current densities. In this basic circuit, the emitter area of Q_2 is eight times that of Q_1. And although both transistors operate at the same current, their current densities are vastly different.*

Fig 4 illustrates the basic operation of a bandgap circuit. In this circuit, the emitter area of Q_2 is eight times that of Q_1. Calculations show that this ratio provides a near-zero TC by generating an optimum difference in current densities (J_1 and J_2) between Q_1 and Q_2. **Ref 1** and **Ref 2** provide a rigorous analysis of these calculations. V_{BE} is the base-emitter voltage of Q_1, and ΔV_{BE}, which appears across R_2, is scaled by the R_1/R_2 ratio to V_1. This voltage has a TC that cancels that of V_{BE}. The op amp raises the V_Z bandgap voltage, which is the sum of V_1 and V_{BE}, to a higher voltage at the output of the reference. This voltage, V_{OUT}, is determined by $(R_4/R_3)+1$ and is usually in the range of 2.5 to 10V, although it can be the bandgap voltage itself.

Designers of IC bandgap references often incorporate additional features to make the devices more flexible. For example, some circuits have terminals brought out from an internal voltage divider, which lets you program a variety of fixed, calibrated voltages, such as 2.5, 5, 7.5, and 10V. You can also use these terminals with external resistors to set arbitrary voltages. Although special-purpose hybrid types are available, most bandgap references are fabricated in the less expensive monolithic form.

Look at the specifications

An ideal voltage reference would have no errors at all. Its output voltage would be initially exact and not vary with time, temperature, input voltage, or load conditions. In the real world, an ideal reference is not possible, and manufacturers provide specifications to let the user know what the expected variations are for a number of key parameters. Of prime importance are the specifications for output voltage error, temperature coefficient, line regulation, load regulation, and long-term stability. You should look at these specifications both individually and collectively to obtain a true picture of a reference's expected performance.

The *output voltage error* is the initial, untrimmed accuracy of the reference at 25°C at a specified input voltage. Specified in millivolts or a percentage, the measurement is normally made using a device that is traceable to a voltage standard. Some references provide pin connections for trimming their initial accuracy with an external potentiometer.

The *temperature coefficient* of a reference is its average change in output voltage as a function of temperature compared with its value at 25°C. Specified in ppm/°C or mV/°C, the TC is independent of variations in other operating conditions.

Zener-based IC references use temperature-compensating diodes and op-amp circuitry to obtain voltage-reference performance.

Line regulation is the change in output voltage for a specified change in input voltage. Usually specified in %/V or μV/V of input change, line regulation is a measure of a reference's ability to handle variations in supply voltage.

Load regulation is the change in output voltage for a specified change in load current. Specified in μV/mA, %/mA, or ohms of dc output resistance, load regulation includes any self-heating effects due to increased power dissipation at high values of load current.

Long-term stability is the change in the output voltage of a reference as a function of time. Specified in ppm/1000 hours at a specific temperature, long-term stability is difficult to verify. As a result, manufacturers usually provide only typical specifications based on device data collected during the characterization process.

Although these specifications are the most important, others, such as *dynamic impedance* and *noise*, may also be of concern. In particular, noise is an important consideration when using a reference with a high-resolution A/D or D/A converter. For example, a 12-bit A/D converter has an LSB weight of about 0.0244% of its full-scale range. For a full-scale range of 10V, the value of the LSB weight would be about 2.44 mV. The noise from the reference should be less than 10% of that value, or less than 244 μV. For a 16-bit converter, the requirement gets even tougher—the LSB weight is about 0.0015% and the reference noise should be less than 15 μV. You need to look carefully at the data sheet to make sure that the specifications you're interested in are well defined. Data sheets for some low-cost references don't always provide information on all possible parameters.

The level of sophistication and pricing for voltage references runs the gamut from simple and inexpensive to complex and costly. Devices are available for, literally, almost any conceivable application.

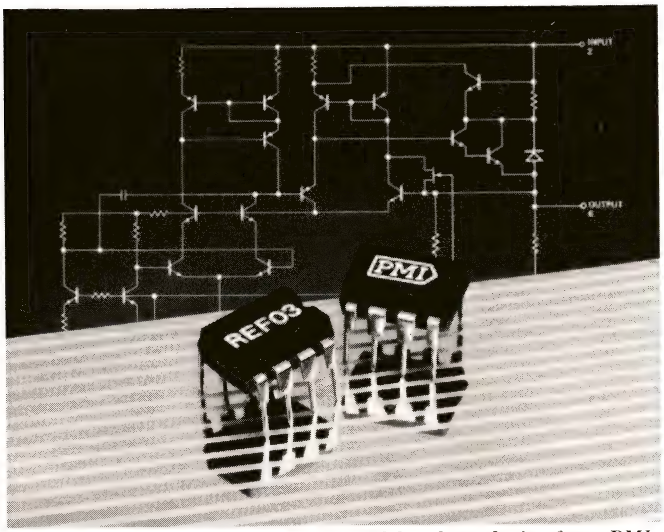
Typical of the lower-cost, general-purpose references is the LM136 series, which is available from companies such as National Semiconductor, SGS-Thomson, and Texas Instruments. Categorized for operation over the military, industrial, and commercial temperature ranges, respectively, the LM136, -236, and -336 are bandgap references with an output voltage of 2.5V and an accuracy of 1 or 2%. These references find application in digital voltmeters, power supplies, and op amp circuitry. They're particularly useful in obtaining a stable reference from a 5V logic supply.

Because the LM136, -236, and -336 operate as shunt regulators, you can use them as either positive or negative references. Characterized for operation at 1 mA, these references have a typical TC of 3.5 mV from −25 to +85°C and 12 mV from −55 to +125°C. A pin connection lets you trim the devices externally for minimum temperature drift. At 25°C, the typical dynamic impedance is 0.2Ω, and long-term stability is ±20 ppm. Available in TO-92, TO-46, and SO-8 packages, commercial and industrial versions range in price from about $0.70 to $1.30 (1000).

Although better known for its power-supply and motion-control circuits, Silicon General also has a modest line of bandgap references. Its SG103 series—equivalent to National Semiconductor's discontinued LM103 series—is available in 13 voltage ratings ranging from 1.8 to 5.6V. Packaged in a low-profile TO-46 metal can, the $12.75 (100) SG103 complies with MIL-STD-883B and is specified for operation over the military temperature range of −55 to +125°C. Primarily used in low-voltage power supplies, the 2-terminal device features a typical TC of −1 mV/°C and a dynamic impedance of 5Ω.

Other manufacturers of bandgap voltage references include Analog Devices, Linear Technology, Maxim Integrated Products, Motorola Semiconductor, Precision Monolithics (PMI), and Teledyne Semiconductor. Many of these companies' references are interchangeable

Many precision references have a 10V output. *The nominal 10.000V output of the REF102 from Burr-Brown features an initial accuracy of ±2.5 mV and a drift of 2.5 ppm/°C over the −25 to +85°C temperature range.*



Low-cost references, *such as this 2.5V bandgap device from PMI, often come in 8-pin plastic DIPs.*

with devices from other manufacturers, and some offer improved performance compared with the original versions. For example, the LT1019 from Linear Technology is a direct and, in many cases, improved replacement for many bandgap references, including the AD580, AD581, REF-01, REF-02, MC1400, MC1401, and LM168.

Available in voltage ratings of 2.5, 4.5, 5, and 10V, the LT1019 is a third-generation device utilizing thin-film technology and wafer-level trimming of both the reference voltage and the output voltage. Typical specifications for the LT1019 include an output voltage error of 0.02%, a TC of 5 ppm/°C, line regulation of 0.5 ppm/V, and load regulation of 0.1 mV/mA. For low-drift applications, you can achieve a TC of less than 2 ppm/°C by operating the LT1019 in a heated mode using its internal resistor and an external amplifier. Available in either an 8-pin metal can or plastic DIP, the LT1019's prices start at $3.90 (100). Applications for this device include A/D and D/A converters, V/F converters, precision regulators, and strain-gauge bridge excitation.

Maxim Integrated Products offers improved replacements for the 10V REF-01 and the 5V REF-02 bandgap references, two standards introduced by PMI. Maxim's 10V MAX674 and 5V MAX675 have a pretrimmed output voltage that is accurate to ±0.15%, compared with ±0.3% for the REF-01 and REF-02. In addition, the load regulation of 0.002%/mA for the MAX674 and MAX675 is somewhat better than that specified for the REF-01 and REF-02. The MAX674 and MAX675 are available in 8-pin metal cans, plastic DIPs, and SO packages; prices start at $4.25 (100).

Designed for large-volume customers who need a precision reference but can't justify a high cost, the REF-03 from Precision Monolithics 2.5V bandgap reference offers good performance at a unit cost of only $1.75 (100). The REF-03 features a typical output voltage tolerance of ±0.2% (±0.6% max) and a typical TC of 10 ppm/°C (50 ppm/°C max). Typical line and load regulation are 0.002%/V and 0.006%/mA, respectively. The REF-03 is available in 8-pin DIPs and 8-pin SO packages.

A companion to the REF-03, the REF-43 operates at a lower supply current (450 μA max vs 1.4 mA max) and offers better performance, albeit at the higher starting price of $3.75 (100). The 2.5V REF-43 features a maximum output voltage tolerance of ±0.05% and a maximum TC of 20 ppm/°C. The REF-43 is available in a variety of package styles, including 8-pin TO-99s, 8-pin DIPs, and 20-pin LCCs.

For very low-cost applications, Teledyne Semiconductor offers its 1.25V TSC04 and 2.5V TSC05 bandgap references. Although these devices provide only moderate performance, they can satisfy many applications and—at $0.70 (100) in a TO-92 plastic package ($0.95 in TO-52 metal)—are cost effective. The TSC04 and TSC05, which can operate over a range of 20 μA to 20 mA, have an output tolerance of 2% and a maximum TC of 50 ppm/°C. By not using thin-film resistors in these devices, Teledyne is able to reduce manufacturing complexity—and cost. Teledyne also offers bandgap references rated at 5 and 10V, which offer tighter specifications at higher costs.

An unusual device, the micropower LT1034 from Linear Technology, combines a 1.2 or 2.5V bandgap reference with a 7V zener-based auxiliary reference in a single package. Operating at 100 μA, the bandgap reference features a 1% initial tolerance, a TC of 20 ppm/°C typ, and a dynamic impedance of 0.5Ω typ. Useful for less demanding applications, the 7V reference has a 5% initial tolerance and a typical TC of 40 ppm/°C. The LT1034 comes in 3-pin TO-46 or TO-92 packages; prices start at $2.15 (100).

Zener-based references

Although bandgap references that can operate from 5V supplies are widely available, zener-based references, which are usually used with analog circuits that operate from 12 to 15V supplies, are just as plentiful. In addition, compared with bandgap references, many

Bandgap references can provide good performance and, because of their low-voltage capabilities, are particularly useful in circuits operating from 5V logic supplies.

zener-based references have superior performance characteristics. Major suppliers of zener-based references include Analog Devices, Burr-Brown, Linear Technology, National Semiconductor, and Precision Monolithics.

Typical of the high-performance possible with zener-based references is the 10V REF102 from Burr-Brown. Available in a range of temperature grades and degrees of precision, the REF102's best incarnation features a maximum initial error of only ±2.5 mV, a TC of 2.5 ppm/°C, line regulation of 1 ppm/V, load regulation of 10 ppm/mA, and noise of only 5 μV p-p from 0.1 to 10 Hz. Moreover, the REF102 achieves its performance without the use of a heater, which results in a quiescent current of only 1.4 mA. The REF102's combination of specifications make this device well suited for use with high-resolution A/D and D/A converters or as an accurate comparator threshold reference. Available in industrial and military temperature grades and in three grades of precision, prices for the REF102 range from $2.75 to $14 (100).

Analog Devices offers a wide range of both bandgap and zener-based precision references as part of its line of data conversion products. Unique among its offerings is the AD689, an 8.192V zener-based reference that bridges the gap between 5 and 10V references. Many data-conversion and analog circuits operate from ±12V supplies, which can vary over a 10% range. However, using a 10V reference when the supply drops to ±10.8V is a marginal situation at best. Before the availability of the AD689, designers were forced to choose between a 5V bandgap reference or a less complete zener reference between 5 and about 7V. The 8.192V AD689 lets designers maximize a circuit's signal swing when operating from 12V supplies.

The AD689 uses an ion-implanted zener diode and

Manufacturers of voltage references

For more information on voltage references such as those discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Analog Devices
1 Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No. 650

Burr-Brown Corp
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No. 651

Cherry Semiconductor Corp
2000 S County Trail
East Greenwich, RI 02818
(401) 885-3600
Circle No. 652

Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 432-1900
Circle No. 653

Maxim Integrated Products
120 San Gabriel Dr
Sunnyvale, CA 94086
(408) 737-7600
Circle No. 654

Motorola Inc
Linear IC Div
7402 S Price Rd, MD-PR340
Tempe, AZ 85283
(602) 897-3840
Circle No. 655

National Semiconductor Corp
Box 58090
Santa Clara, CA 95052
(408) 721-5000
Circle No. 656

Precision Monolithics Inc
Box 58020
Santa Clara, CA 95052
(408) 727-9222
Circle No. 657

SGS-Thomson Microelectronics
1000 E Bell Rd
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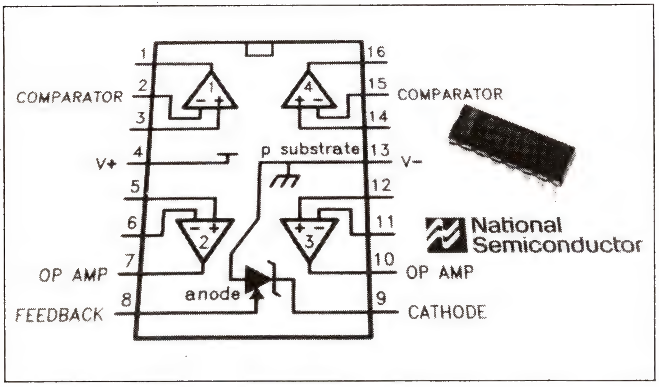
For applications requiring very low drift, you can use some references in a heated mode.



Exemplifying a trend to higher integration, *this IC from National Semiconductor contains an adjustable 1.2 to 6.3V reference in addition to dual op amps and dual comparators.*

laser-trimmed thin-film resistors to obtain its high precision. The part features an initial accuracy of ±4 mV and a TC of 5 ppm/°C, and its 8.192V rating provides a convenient 2-mV/LSB scaling for 12-bit converters. Other specifications include a line regulation of ±200 μV/V max, load regulation of 100 μV/mA max, and noise of 2 μV p-p typ from 0.1 to 10 Hz. Long-term stability is typically 15 ppm/1000 hours. For applications requiring higher initial accuracy, the AD689 provides connections for fine trimming the output to 8.000V. In addition, force and sense connections allow remote sensing of load and ground variations. Available in 8-pin ceramic DIPs, prices range from $2.95 to $25 (100), depending on accuracy and temperature range.

If your application requires maximum performance and cost is no object, you may want to check out the LTZ1000, a 7.2V zener-based reference from Linear Technology. The LTZ1000, which requires external circuitry to set the operating currents, incorporates a subsurface zener, a heater resistor for temperature stabilization, and a temperature-sensing transistor. Designed for use in standard cells, calibrators, and precision voltmeters, the LTZ1000 features a thermal drift of 0.05 ppm/°C, about 1.2 μV p-p of noise, and long-term stability of 2 μV per month. Packaged in an 8-pin metal can, the LTZ1000 operates over the temperature range of −55 to +125 °C and costs $35.50 (100).

Stand-alone IC references will continue to dominate many applications, but there's a gradual, definite trend toward incorporating voltage references in other circuits—notably A/D and D/A converters. In addition, at least one company has incorporated adjustable references in monolithic building blocks containing op amps and comparators.

For example, over the course of the past year, Maxim Integrated Products has introduced a family of 12-bit A/D converters that include either bandgap or zener references. Analog Devices, among others, offers a wide range of A/D and D/A converters with on-chip references. And National Semiconductor recently introduced several monolithic chips containing single, dual, or quad op amps and a voltage reference.

The main advantage of this higher level of integration is convenience. The designer is freed from the task of matching a specific reference to a particular converter or op amp. In addition, there are advantages in cost and board space. Manufacturers can often include an on-chip reference with little penalty in chip real estate and no change in packaging. For many applications in which a reference is needed, this approach offers a cost-effective alternative. EDN

References

1. *Analog-Digital Conversion Handbook*, edited by Daniel H Sheingold, Analog Devices Inc, Prentice-Hall, Englewood Cliffs, NJ, 1986.

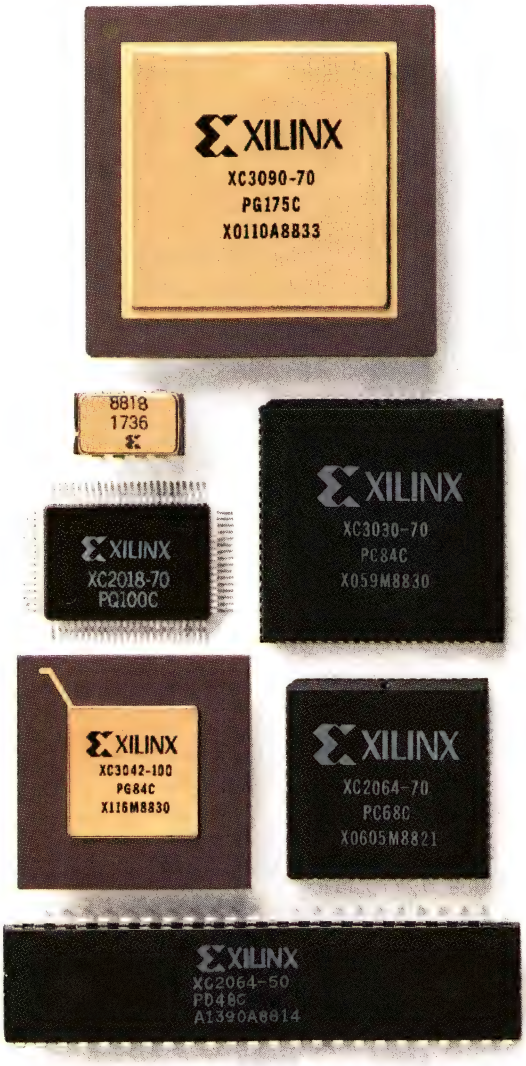
2. Knapp, Ron, "Selection criteria assist in choice of optimum reference," *EDN*, February 18, 1988, pg 183.

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

WHAT'S COMING IN EDN

EDN Magazine's February 1, 1990, issue will feature a staff-written Special Report about add-on buses. Part 3 of the designer's guide to flash-ADC testing concludes this design series with a discussion of the measurements you'll need to fully characterize flash A/D converters. Also, Contributing Editor Bill Travis looks at analog comparators that address TTL and ECL ICs. Be sure to look for our regular departments.

IT HAS TO BE GOOD. OUR NAME IS ON IT.



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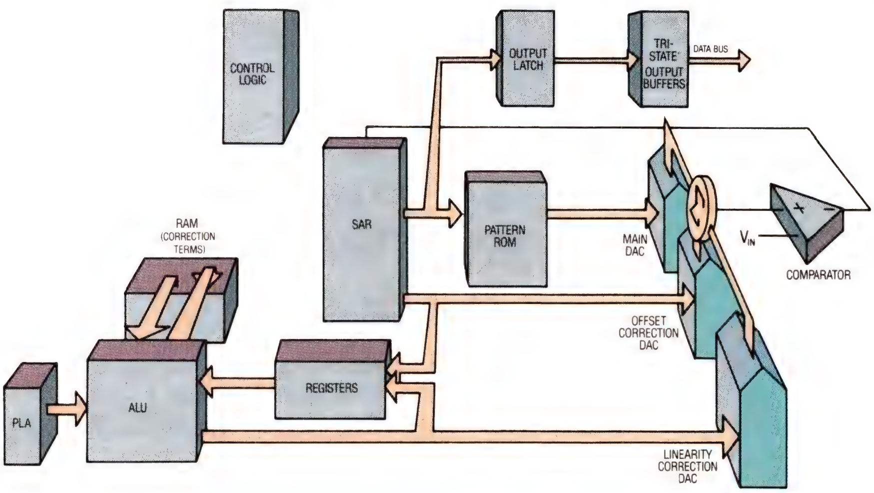

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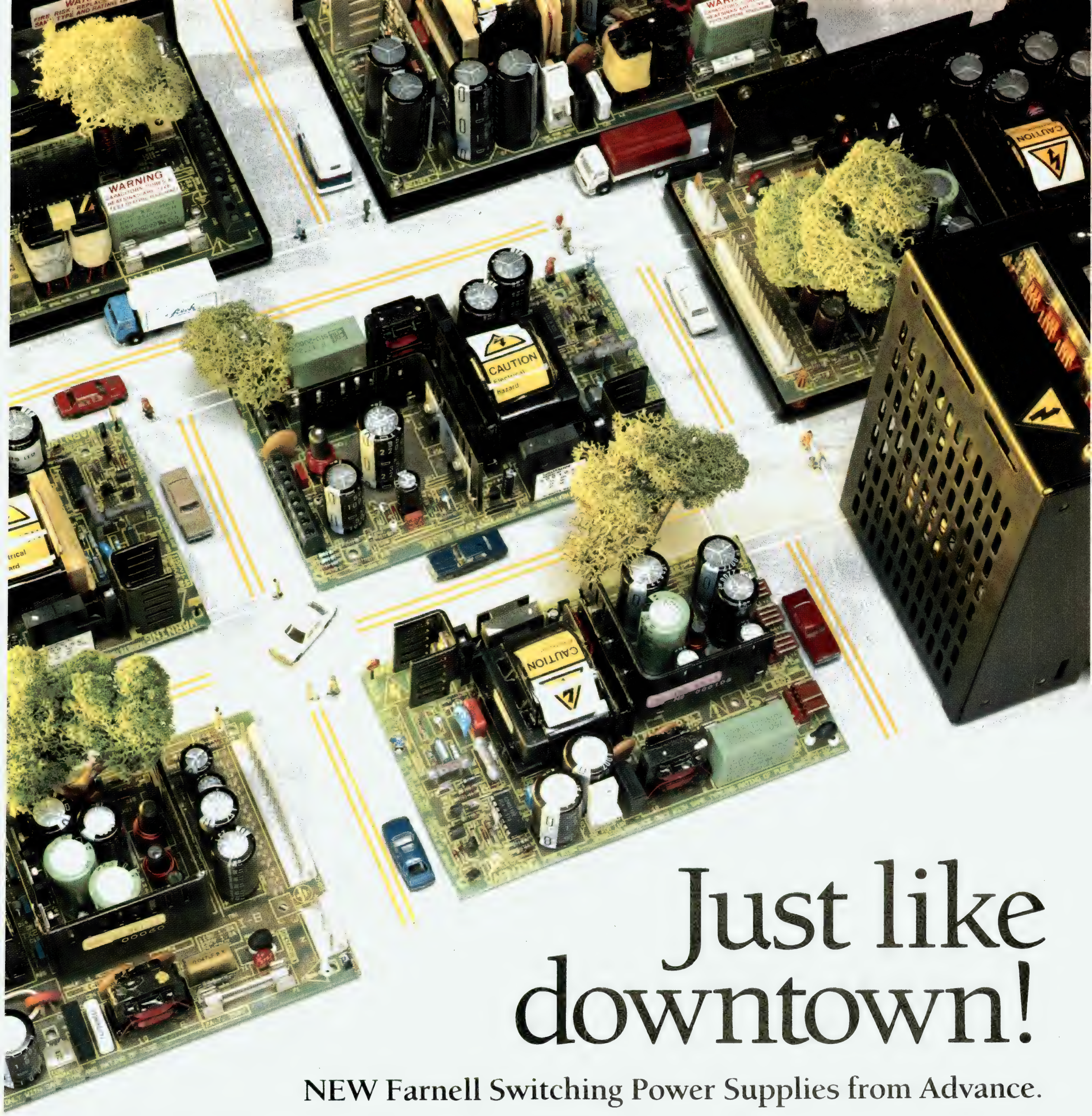
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DESIGNER'S GUIDE

flash–ADC testing
Part 2

DSP test techniques keep flash ADCs in check

By testing your flash A/D converter, you can ensure that it's faithful to all the specifications listed on its data sheet. Part 2 of this 3-part series presents a number of methods, including sine-wave curve fitting and the FFT, that you can use to test flash converters. Readily available benchtop instruments or personal computers are the only equipment that you'll need to use these methods.

Walt Kester, *Computer Labs Div, Analog Devices*

It's important to know how your flash A/D converter will perform in real-world applications. Therefore, you may want to perform any one of a variety of tests on your converter to determine its deviation from ideal performance. As Part 1 of this series discussed, flash ADCs exhibit errors due to static and dynamic nonlinearities, and these errors increase as the input signal's slew rate increases. Thus, the actual S/N ratio will fall short of the converter's theoretical value. Even if you don't apply these tests yourself, becoming familiar with them will help you evaluate data-sheet specifications more accurately, because many manufacturers use these same methods.

Another reason you may want to test your flash converter is to gain information that the manufacturer doesn't provide. Specifications such as S/N ratio and its related effective number of bits are key in all applications and are normally specified, but other specifications that are more important for your particular application may not be included on the data sheet. For example, video designs typically require that you know a converter's differential phase and gain (**Ref 1**). Communications systems may even depend on esoteric specifications such as the spurious-free dynamic range, which isn't available on many data sheets.

For a full-scale sine-wave input, the theoretical rms-signal to rms-quantization noise ratio is

$$\text{S/N RATIO} = 6.02N + 1.76 \text{ dB},$$

where N equals the number of bits (**Ref 2**). The rms quantization-noise voltage for an ideal ADC within the Nyquist bandwidth is $q/\sqrt{12}$, where q is the weight of the LSB expressed in volts.

The most popular method for extracting a flash converter's S/N ratio and effective number of bits is through discrete Fourier transforms (DFTs). Today, you can perform sophisticated DSP tests with PC-based test systems and standard software packages. The test system in **Fig 1**, for example, can execute a 1024-point FFT in less than one second. Most of the hardware you'll need is available as plug-in boards for the PC. However, you'll have to do a fair amount of work before you can begin to use a PC-based test system. First, you'll need to design a high-speed buffer-memory board to capture the data from the flash

DSP test techniques determine your converter's deviation from ideal performance, and they even tell you certain specifications that the ADC's data sheet doesn't.

ADC. Typically, you'll need to use high-speed static CMOS or ECL RAMs. Second, plan to design an appropriate logic interface to connect this buffer memory to the digital I/O card of the PC.

Another hardware feature you might consider is an evaluation board, which certain manufacturers of video-speed ADCs supply to ease design testing. Many evaluation boards contain reference voltages, power-supply decoupling, timing circuits, output registers, and connectors. The evaluation boards usually have a matching reconstruction DAC. In most cases, the manufacturer has optimized the design of these boards so that your ADC test won't be corrupted by faulty or poorly designed support circuits.

Your software must include a program to capture the data and then load it into the memory of the PC. If you plan to use FFT analysis, you must link a standard FFT software package to your test program. You may also have to generate a look-up table to store any special weighting functions required by your particular sampling scheme. Also, adding a coprocessor card will speed up the thousands of multiplications that FFT-based analysis requires.

If you don't have the time or the energy to build your own test system, consider one of the benchtop instruments available from a number of instrumentation manufacturers. These turnkey systems typically utilize a high-speed logic analyzer to capture data. Because menu-driven software allows you to select from a variety of tests, you incur practically no hardware or software development time.

To test a flash ADC using Fourier analysis, you must apply a spectrally pure sine wave to the converter and store a number of contiguous output data samples. Then, using DFT techniques, your test program calculates the rms-signal and rms-noise content and determines the ratio of the two. Noise calculations using DFT techniques include not only the converter's quantization noise but also the harmonics of the input sine wave. In addition, harmonics that fall outside the Nyquist bandwidth are aliased back into the Nyquist bandwidth because of the sampling process. Thus, to achieve accurate and repeatable results, the purity of the sampling clock and the input sine wave is critical.

You can use either coherent or noncoherent sampling to evaluate the ADC performance. Coherent sampling simply means that your record of samples contains an integer number of sine-wave input cycles. Alternatively, noncoherent sampling produces a record that contains noninteger multiples of the input. You must choose between these sampling schemes based on the type of input data you expect. Coherent testing is more suited to a laboratory environment when you know the precise frequency content of an input signal, and it requires careful attention in the selection of the input and sampling frequencies. Noncoherent testing yields a better representation of ADC performance in a real-world application such as spectral analysis, because

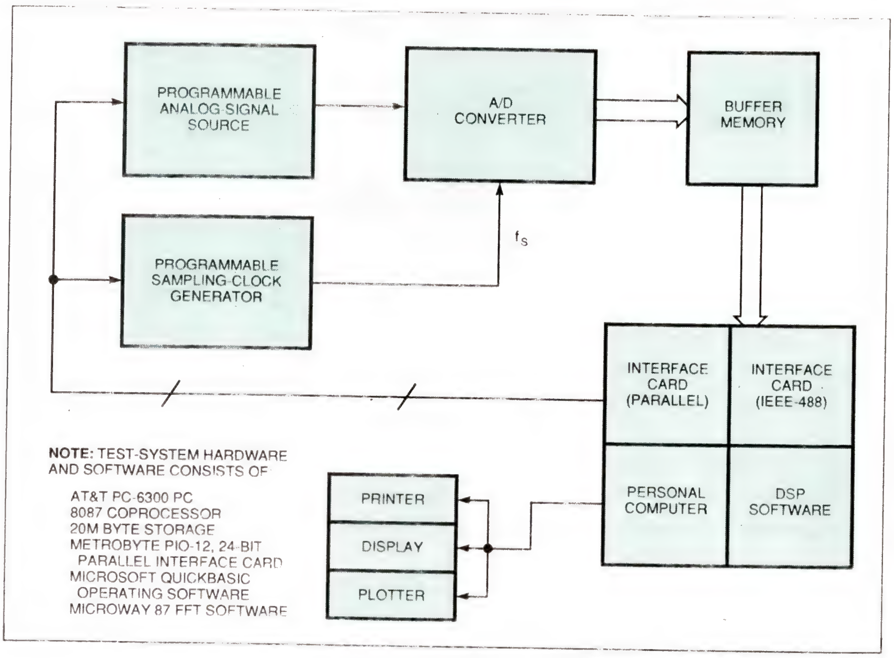

***Fig 1**—This DSP test system for a flash ADC can execute a 1024-point FFT in less than one second, but the system requires a significant design effort. Hardware requirements include a high-speed buffer memory and logic interface between this memory and your PC. Software requirements include a program to capture the data and load it into the memory of the PC, as well as a link between your test program and a standard FFT software package.*

the precise frequency content of the signal being digitized is a mystery.

However, whenever the number of time samples doesn't contain an integer number of input cycles (noncoherent testing), you'll have to time-weight the samples to reduce frequency side lobes. Without weighting, discontinuities will cause the main lobe's energy—the fundamental—to leak into many other frequency bins. The term "bins" refers to the spaces between spectral lines or spectral peaks. The number of bins for a particular spectrum equals the sampling frequency divided by the record length, or f_S/M. The leakage of the signal from the central bin to side-lobe bins makes accurate spectral measurements impossible—you simply can't distinguish the frequency bins that contain actual signal information from those that contain noise. Another reason to time-weight the samples is that the end user of your A/D-conversion system may be interested in the performance of the ADC using an identical or similar window.

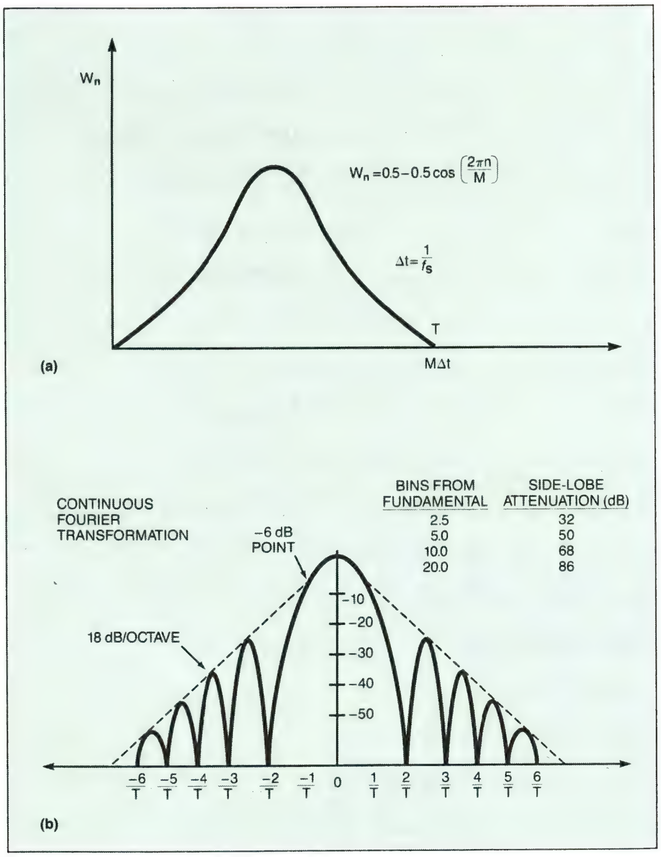

Fig 2—When the record of samples doesn't contain an integer number of input cycles*—that is, when you're using noncoherent sampling—you must precondition the data with a weighting function. The Hanning window shown here in the time domain* ***(a)*** *and the sampled-frequency domain* ***(b)*** *is a popular weighting function.*

Noncoherent sampling involves fewer input- and sampling-frequency restrictions than coherent sampling does, but it requires careful attention in the selection and use of the weighting function. Also, to prevent masking out harmonics of the fundamental, avoid using inputs that are integer submultiples of the sampling frequency. If your input frequency is an integer submultiple of the sampling frequency, the quantization noise, $q/\sqrt{12}$, will be concentrated in the harmonics of the input frequency rather than uniformly distributed across the Nyquist bandwidth. Ultimately, this condition leads to incorrect harmonic-distortion test results.

One popular weighting function is the Hanning window **(Ref 3)**, which is described by the equation

$$W_n=0.5-0.5\cos\left(\frac{2\pi n}{M}\right),$$

where W_n is the weighting coefficient for the nth data sample, and M is the total number of samples. **Fig 2** graphically depicts the Hanning window in both the time and the frequency domains.

To calculate the S/N ratio, you have to decide the number of frequency bins to include in the fundamental and the number of bins to consider as noise. As **Fig 2** shows, you can correlate the amount of side-lobe attenuation with the lobe's distance, in terms of bins, from the fundamental bin. **Fig 2b** includes a table that lists some of these values. You'll have to make your decision based on the theoretical S/N ratio of the converter you're testing.

For example, an 8-bit converter has a theoretical, maximum S/N ratio of approximately 50 dB. In order to ensure that the side-lobe energy doesn't cause an artificially high noise measurement (and hence an artificially low S/N-ratio measurement), you should include at least 10 frequency bins on either side of the fundamental when calculating the signal level. (Simply take the square root of the sum of the squares of all 21 bins as your signal level.) Now, any side-lobe energy outside this region will be at least 68 dB below the fundamental signal level (18 dB below the theoretical, 8-bit quantization noise floor of 50 dB), and side-lobe leakage won't significantly affect the accuracy of your S/N-ratio measurement.

Other weighting functions may better suit your application. For example, **Fig 3** compares the popular

Today, you can perform sophisticated DSP tests with PC-based test systems and standard software packages.

Hanning window's spectral representation with the more sophisticated, minimum 4-term, Blackman-Harris type. For the same record length, the Blackman-Harris window provides better spectral resolution than the Hanning window, making it more suitable for critical spectral analysis, such as measuring 2-tone, third-order intermodulation-distortion products. The extra computations for the Blackman-Harris window don't lengthen processing time, because you calculate them only once and store them in a look-up table.

As previously stated, you can use coherent sampling if you know the characteristics of your input signal and if you choose the sampling rate accordingly. Coherent sampling eliminates leakage and the need for windowing (**Ref 4**); the spectral result of a coherently sampled signal is simply a single-frequency peak. Certain restrictions apply to the choice of the sampling rate and

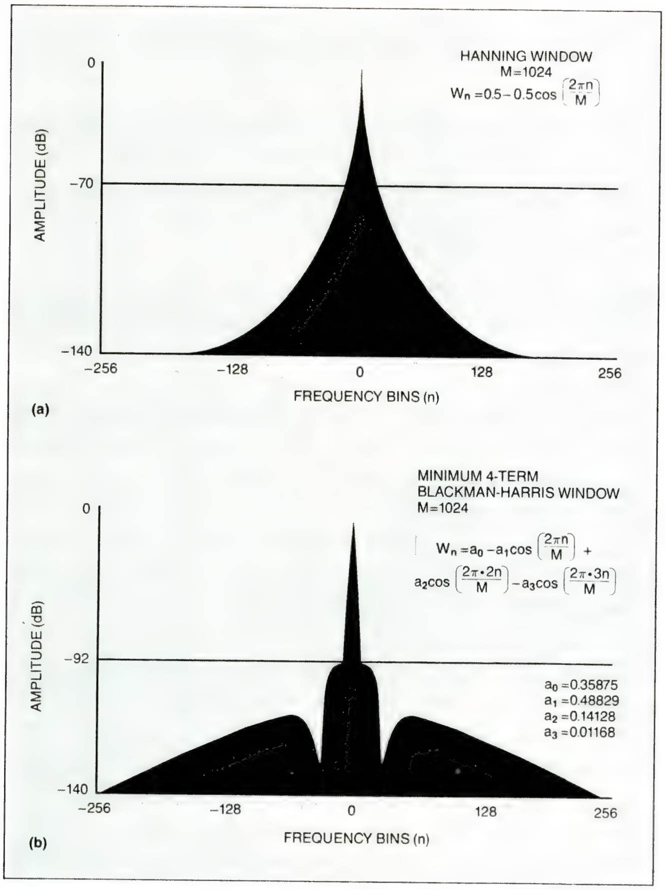

Fig 3—The Blackman-Harris windowing function (b) *resolves closer peaks in a frequency spectrum than does the Hanning window* ***(a)****. The mathematical expression for the Blackman-Harris window is more complex, but you only need to calculate the terms once and then store them in a look-up table.*

the sine-wave frequency, however. First, you must observe the following ratio:

$$\frac{f_{in}}{f_S} = \frac{M_C}{M}.$$

M_C equals the number of integer cycles of the sine wave during the record period. For a whole number of cycles, M_C must be an integer. To ensure that you don't take repetitive data, M_C should also be a prime number: 1, 3, 5, 7, 11, 13, 17, etc. By using prime numbers, you ensure that all samples during the record period are unique. When using coherent sampling, it's mandatory that the ratio M_C/M be constant. This requirement implies that you derive f_S and f_{in} from two locked frequency synthesizers.

Calculate the DFT

After selecting the record length and determining the weighting function (for noncoherent sampling), you must write your DFT test program. Your program must find the DFT of the sequence of weighted data samples for M/2 frequencies (the Nyquist frequency). Thus, the program should solve the following two equations for the kth frequency:

$$A_k = \frac{1}{M}\sum_{n=1}^{M} W_n D_n \cos\left[\frac{2\pi k(n-1)}{M}\right]$$

$$B_k = \frac{1}{M}\sum_{n=1}^{M} W_n D_n \sin\left[\frac{2\pi k(n-1)}{M}\right].$$

In these equations, A_k and B_k represent the magnitudes of the cosine and sine parts of the kth spectral line; n is the number of time samples; W_n is the weighting function; D_n is the amplitude of the time-function data point; and k is the number of a spectral line. The total magnitude of the kth spectral line is

$$MAGNITUDE_K = \sqrt{A_k^2 + B_k^2}.$$

The program's results yield M/2 components, which are the frequency-domain representation of the M time samples. The resolution or spacing between the spectral lines, Δf, equals f_S/M and is the bin size or bin width.

Typically, you should select the number of time samples (M) to be between 256 and 4096, depending on

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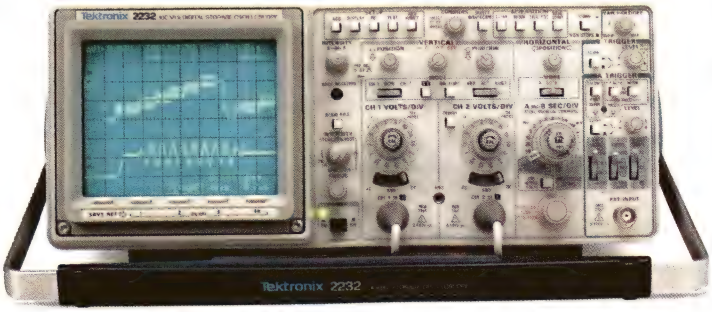

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The discrete Fourier transform is the most popular method for determining a converter's true S/N ratio and effective number of bits.

the desired resolution and the size of the buffer memory. M must be equal to an integer that's a power of two. If you're using noncoherent sampling, you can compress leakage around the main lobe by using a larger record length, thereby leaving a larger percentage of the Nyquist spectrum uncontaminated. For example, the Hanning weighting leakage is ±10 bins from the fundamental for 68-dB side-lobe suppression. If the record length is 256, then the leaky fundamental occupies 20 bins out of 128 spectral components, or 16% of the digital spectrum. When M equals 1024, the percentage reduces to 20/512, or 4%.

In practice, you can use one of the many FFT algorithms to simplify and speed the DFT calculations (**Ref 5**). An FFT algorithm will produce the same results as the DFT equations above, and the computation time is much faster.

Verify the FFT

Consider the noise floor when verifying the FFT. Assuming that the round-off error contributed by the DSP-noise calculation (the error caused by using a finite number of bits in the FFT multiplications and additions) is negligible, the rms-signal to rms-noise level in a single frequency bin of width Δf is

$$\text{S/N RATIO}_{\text{FFT}}=6.02\text{N}+1.76\text{ dB}+10\text{ LOG}_{10}\left(\frac{\text{M}}{2}\right).$$

This equation represents the FFT noise floor. You should choose M so that any spurious components you want to resolve lie at least 10 dB above this floor.

Basic software can easily generate an ideal N-bit sine wave by using the Integer (INT) function to truncate the value to the proper resolution. For instance, an input signal of frequency f_{in} is equal to

$$V_q=V_O \sin\left(\frac{2\pi n f_{in}}{f_S}\right),$$

where n is the nth time sample for an ADC that has infinite resolution. You can calculate the corresponding quantized value using

$$V_q(n)=\text{INT}\left(\frac{V_O \sin \frac{2\pi f_{in}}{f_S}}{q}\right),$$

where $q=2V_O/2^N$. Substituting this expression for q in the above equation yields

$$V_q(n)=\text{INT}\left[2^{N-1}\sin\left(\frac{2\pi n f_{in}}{f_S}\right)\right].$$

The INT function simply truncates the fractional portion of $V_q(n)$.

To check the dynamic range of the FFT, calculate the S/N ratio by using 6.02N+1.76 dB for increasing values of N and observing the point at which the S/N ratio no longer increases by 6.02 dB/bit. The sine-wave input to the weighting function and the FFT are more ideal as N approaches infinity. By making N arbitrarily large, you can greatly reduce quantization-error effects and analyze the true noise floor of the FFT. You can also examine the characteristics of the weighting function.

Match the sine wave to a curve

Another test method to use with flash ADCs is sine-wave curve fitting. You perform this test after the ADC digitizes the sine wave and after your test system stores the data in its memory. A record length of 1024 samples is usually sufficient. The software then calculates the best-fit, ideal N-bit sine wave to match the data points, based on the sine wave's amplitude, offset, frequency, and phase required to minimize the rms error between the actual and the ideal sine wave (**Refs 6** and **7**). This method also requires that the input sine-wave frequency contains no subharmonics of the sampling rate. If you know the precise sine-wave frequency, the curve-fit algorithm is much simpler than the FFT method, and the probability that the algorithm will converge is higher.

After the software computes the rms error, Q_A, between the ideal sine wave and the actual sine wave, you can calculate the effective number of bits by using

$$\begin{matrix}\text{EFFECTIVE}\\ \text{NUMBER OF BITS}\end{matrix}=N-\text{LOG}_2\left(\frac{Q_A}{Q_T}\right),$$

where Q_T is the theoretical rms quantization error, $q/\sqrt{12}$. This measurement includes errors due to differential nonlinearity, integral nonlinearity, missing codes, aperture jitter, and noise, in addition to the quantization noise.

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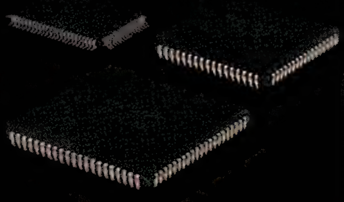

NEC

Coherent testing is more suited to a laboratory environment; noncoherent testing more closely represents ADC performance in the real world.

The effective number of bits that you calculate using the sine-wave curve-fitting method correlates with the value of the full-scale, FFT S/N-ratio measurement obtained using the equation

$$\text{EFFECTIVE NUMBER OF BITS} = \frac{\text{S/N RATIO}_{\text{ACTUAL}} - 1.76\text{ dB}}{6.02}.$$

However, if you measure the effective bits of a sine-wave input signal whose amplitude is less than full scale, you must include the following correction factor in the above equation to achieve correlation between the two methods:

$$\text{EFFECTIVE NUMBER OF BITS} = \frac{\text{S/N RATIO}_{\text{ACTUAL}} - 1.76\text{ dB}}{6.02} + \frac{\text{LEVEL OF SIGNAL BELOW FULL SCALE (dB)}}{6.02}.$$

One useful method for reducing the effects of the D/A converter in making gross back-to-back measurements on an ADC is the beat-frequency method. **Fig 4** illustrates a basic test setup. This test method stresses the converter with a near-Nyquist signal and drives the converter at its maximum sampling rate. Thus, the analog-input sine wave should be slightly lower in frequency than half the sampling frequency. The test system updates the registers that drive the DAC at an even submultiple of the sampling rate, f_S/N, where N is a power of 2. (N is not the ADC's resolution.) The resulting signal from the DAC is a low-frequency sine wave whose exact frequency equals the difference between half the sampling rate and the analog-input frequency. As **Fig 4** shows, you should clock the DAC at a much lower rate, f_S/N—known as the decimation rate—thereby reducing the effects of glitches and other dynamic errors.

You can use the beat-frequency method to make signal-to-noise measurements over the Nyquist bandwidth, $f_S/2N$. You also can examine the low-frequency beat on an oscilloscope for missing codes and other nonlinearities. To measure the harmonic content of the beat frequency, you can use a low-frequency spectrum analyzer. The harmonics of the low-frequency beat are directly related to the harmonics of the analog-input frequency. A beat frequency of a few hundred kilohertz works well. To prevent jitter on the low-frequency beat signal, you must derive both the analog-input sine wave and the sampling frequency from frequency synthesizers or crystal oscillators.

This beat-frequency test is also effective in measuring the flash converter's performance for input signals near the sampling frequency. The performance under these conditions is useful for radar in-phase and quadrature-phase systems and in IF-to-digital conversion. To perform this test, set the ADC's analog-input frequency to slightly less than the sampling rate. The circuit generates a low-frequency beat even if the DAC updates at the sampling rate. However, updating the DAC at f_S/N reduces the effects of DAC dynamic errors on the measurements.

You can use DSP techniques and FFTs to analyze **Fig 4**'s decimated data for a wide range of input frequencies. You do have to remember the rules of aliasing, however, to know where to expect the funda-

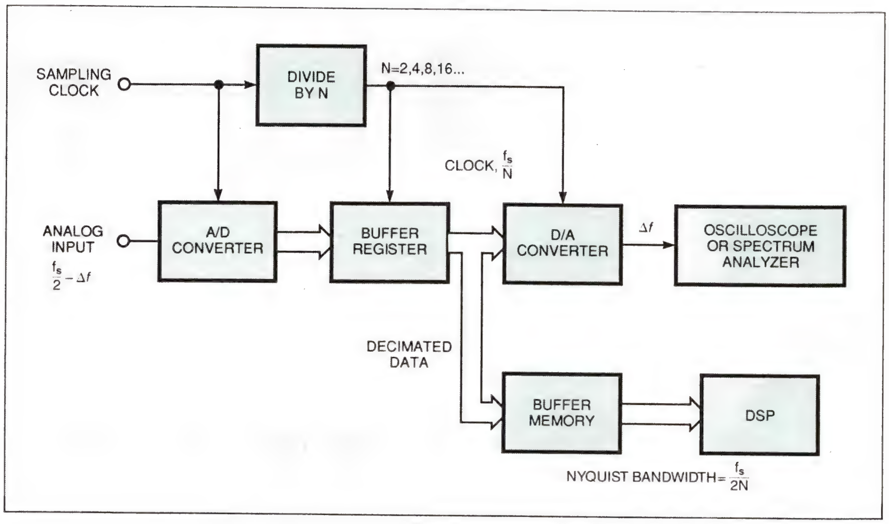

Fig 4—The beat-frequency test stresses the converter with a near-Nyquist input signal, *and it drives the converter at its maximum sampling rate. You can then examine the low-frequency beat on an oscilloscope and search for missing codes and other nonlinearities.*

mental signal to show up in the FFT output spectrum. You may think your FFT is sampling your signal at a rate of f_S/N, but the converter is actually sampling at a rate of f_S.

Once you understand how to use these various techniques, you can start to probe your particular converter to measure its real performance. Part 3 will discuss how you apply these techniques to actually test an ADC in your system and determine a number of static and dynamic specifications. **EDN**

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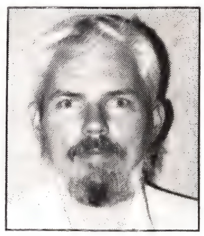
Author's biography



Walt Kester is a technical-support manager for the Computer Labs division at Analog Devices. Walt has been with the company for 20 years and supports the development of high-speed ADCs, DACs, S/H amplifiers, and op amps. He has a BSEE from North Carolina State University and an MSEE from Duke University. In his spare time, Walt enjoys carpentry and travel.

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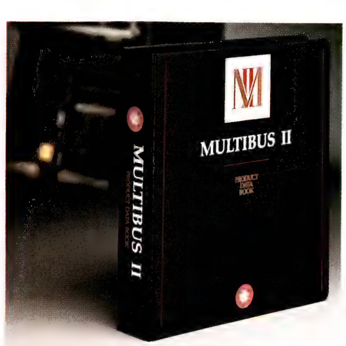

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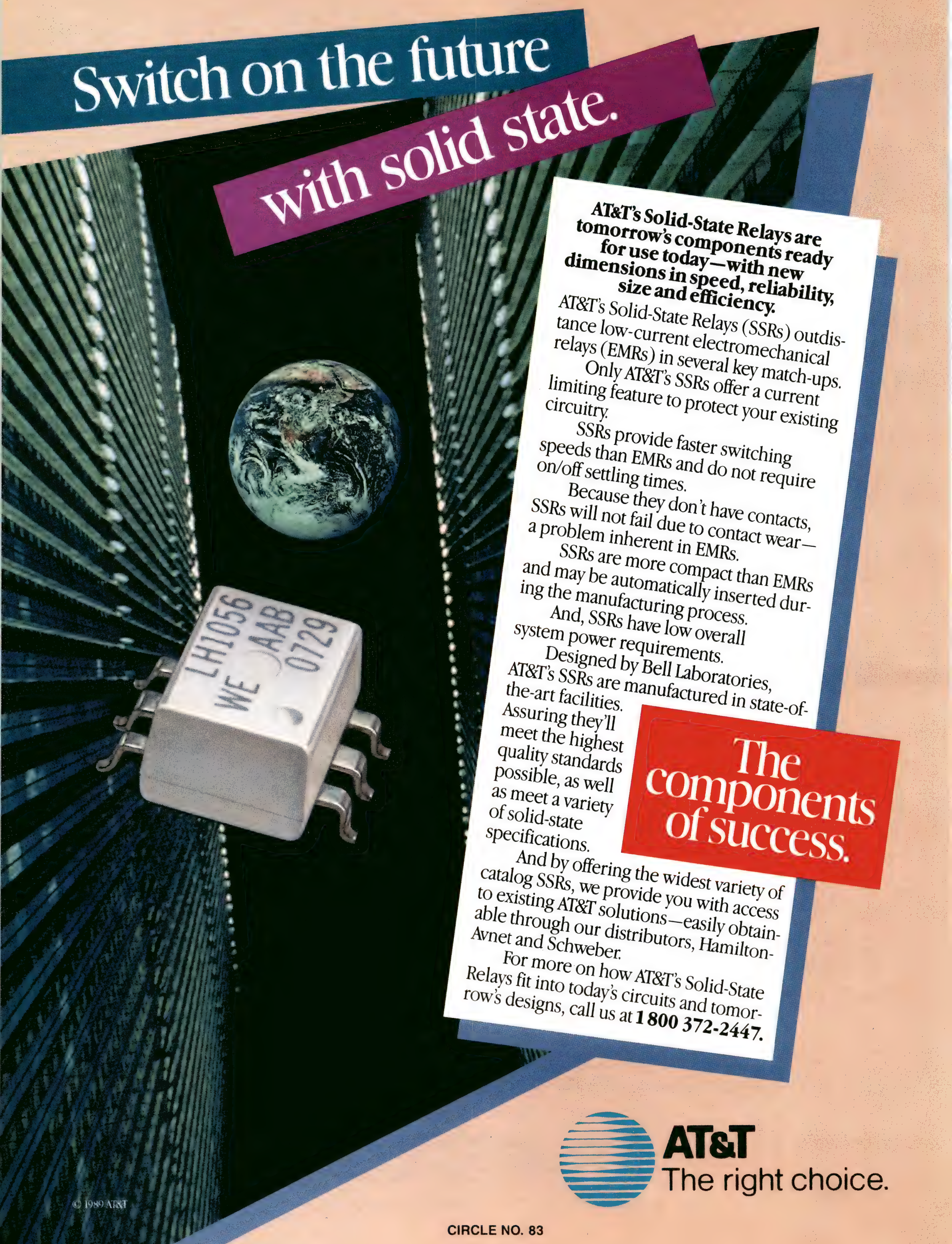
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CIRCLE NO. 83

Basic principles and ingenious circuits yield stout switchers

A substantial percentage of power supplies are step-down regulators. Although the theory of step-down, "buck" switching regulators is well established, myriad practical details, if mishandled, can spoil the theory's pristine beauty. Luckily, convenient, easily applied switching-regulator ICs have recently become available.

Jim Williams, *Linear Technology Corp*

To design a step-down switching regulator, you can't just copy a circuit from a data sheet or use a theoretical method from a book. Designing step-down switching regulators means solving a nettlesome host of problems and properly following some basic principles.

By far, the toughest nuts to crack are the magnetic components. Magnetic components account for probably 90% of the problems in switching-regulator design. Because of the overwhelming level of difficulty associated with magnetic components, you must choose them judiciously.

The most common magnetic-component problem is saturation. An inductor saturates when it cannot support any more magnetic flux. As an inductor saturates, it begins to look more resistive and less inductive. When it's saturated, only the inductor's dc copper resistance and the source's capacity limit current flow. Thus, saturation often results in destruction.

Although you could apply electromagnetic theory (**Ref 1**), practically speaking, an empirical approach is often the best way for you to select inductors. A practical approach involves real-time analyses using the ultimate simulator—a breadboard. If you desire, you can use inductor-design theory to augment or confirm your experimental results.

Fig 1 shows a typical step-down switching regulator. The #845 inductor kit from Pulse Engineering (San Diego, CA) proves useful at the breadboard stage. **Fig 2a** shows the results of installing a 450-μH, high-capacity-core inductor in **Fig 1**'s circuit and the circuit running at its intended voltage and current levels. Trace A is the regulator-IC V_{SW} pin's voltage; trace B shows its current. When V_{SW} is high, inductor current flows. This particular inductor's high value results in the current rising relatively slowly. The circuit's behavior is linear, indicating that no saturating is occurring.

Fig 2b shows the results of installing a lower-value unit. Although the current rises at a steeper rate, the inductor does not saturate. **Fig 2c** shows a still lower inductance. Here the current ramp is quite pronounced, but still well controlled. **Fig 2d** brings some informative surprises. This high-value unit, wound on a low-capacity core, starts out well but saturates rapidly; it is clearly unsuitable.

Trying out different inductors this way quickly narrows your choice to a range of devices. Several may produce acceptable results. You could further select

Magnetic components account for probably 90% of the problems in switching-regulator design.

the optimal unit on the basis of other parameters, such as cost, size, and operating temperature. A standard device may suffice, or the inductor manufacturer can supply a customized version.

The invasion of the drawer dwellers

An alternate inductor-selection method exists—one favored by those who have no inductor kit, time, or adequate instruments. You can use this alternate method when faced with an immediate deadline and a drawer full of inductors of unknown or questionable lineage. Confronting these challenges, engineers often simply insert one of these drawer dwellers into an unsuspecting circuit.

Although this method's theoretical underpinning is perhaps questionable, its seemingly limitless popularity compels coverage. At Linear Technology, we've developed a 2-step procedure for screening inductors of unknown characteristics. Inductors passing both stages of the test have an excellent chance (75%—based on a sample of randomly selected inductors) of performing adequately in a prototype circuit. The only instruments required are an ohmmeter and a scale.

The first test consists of weighing the candidate inductor. Acceptable limits range between 0.01 and 0.25 lbs. The second test involves measuring the inductor's dc resistance. Acceptable limits are usually between 0.01 and 0.25Ω.

When using an inductor selected by this method, by all means try low power first, then gradually increase loading. As you increase loading, observe the inductor's and regulator chip's heating, making sure that their dissipation is no more than warm to the touch. Disproportionate heat increases as you increase the load probably indicate that the inductor is saturating. Either reduce the load or go back to the drawer and try again.

Capacitors require consideration

Think carefully about your capacitors' requirements, as you must account for all operating conditions. Though voltage rating is the most obvious consideration, remember to also plan for the effects of the capacitors' equivalent series resistance (ESR) and inductance. These specifications can have significant impact on your circuit's performance. In particular, an output capacitor with high ESR can make compensating the loop difficult or decrease efficiency. Other considerations are layout, diode breakdown, and switching requirements.

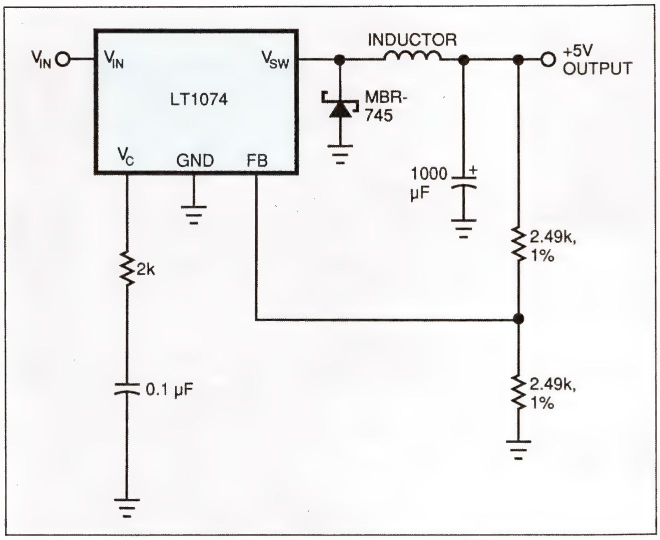


Fig 1—You can use a typical switching-regulator *circuit to sample candidate inductors.*

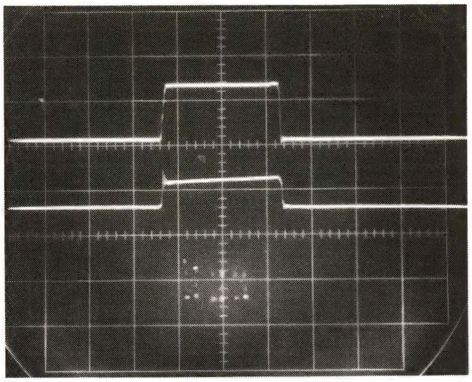
Layout is vital. Don't mix signal, frequency-compensation, and feedback returns with high-current returns. Arrange the grounding scheme for the best compromise between ac and dc performance. In many cases, a ground plane may help. Account for possible effects of stray flux from the inductor or other components and plan your layout accordingly.

You must think through diodes' breakdown and switching ratings and account for all operating conditions. Transients usually cause the most trouble for diodes, introducing stresses that are often hard to predict. Study the datasheet's breakdown, current capacity, and switching-speed ratings carefully. Ask yourself if these specifications were determined under the same conditions as those in your circuit. If in doubt, consult the manufacturer.

Switching diodes have two important transient characteristics: reverse-recovery time and forward turn-on time. Reverse-recovery time occurs because the diode stores charge during its forward-conduction cycle. This stored charge causes the diode to act as a low-impedance conductive element for a short period of time after reverse drive is applied.

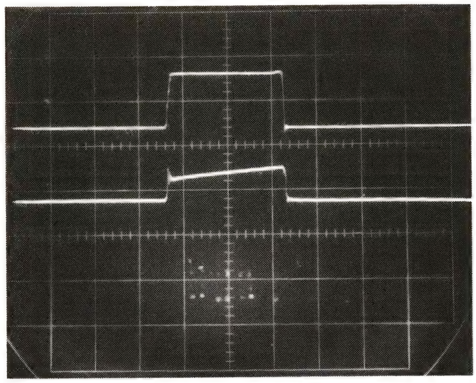
Hard turn-off diodes switch abruptly from one state to the other following reverse-recovery time. They therefore dissipate very little power, even with moderate reverse-recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can dissipate considerable power during the turn-off interval.

Even fast diodes can be useless if stray inductance



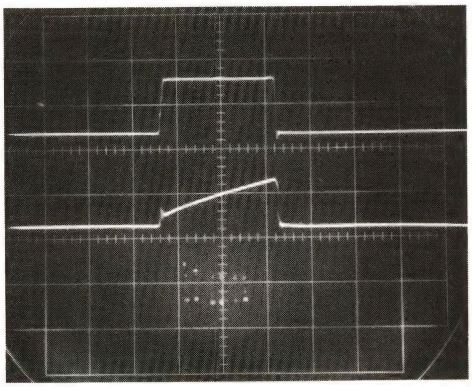
(a) HORIZONTAL SCALE=2 μSEC/DIV

TRACE	VERTICAL
A	10V/DIV
B	1A/DIV



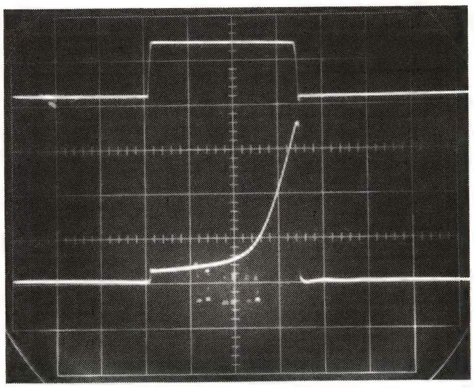
(b) HORIZONTAL SCALE=2 μSEC/DIV

TRACE	VERTICAL
A	10V/DIV
B	1A/DIV



(c) HORIZONTAL SCALE=2 μSEC/DIV

TRACE	VERTICAL
A	10V/DIV
B	1A/DIV



(d) HORIZONTAL SCALE=2 μSEC/DIV

TRACE	VERTICAL
A	10V/DIV
B	1A/DIV

***Fig 2—After installing a 450-μH,** high-capacity-core inductor in the test circuit the waveforms in **(a)** result: Trace A is the regulator-IC V_{SW} pin's voltage; trace B is its current waveform. A lower-value, 170-μH inductor produces these waveforms **(b)**. After installing an even lower-value, 55-μH inductor, the current ramp becomes quite pronounced **(c)**. In **(d)**, a 500-μH, low-capacity-core inductor plainly has too low a value because the current waveform shows that the inductor has quickly saturated.*

in the diode, output capacitor, or control loop is high. Remember that 20-gauge hook-up wire has 30 nH/in. of inductance. Currents switching on the order of 10 A/sec are typical in regulator circuits. These fast-changing currents can easily generate several volts/in. across the wiring's stray inductance. Keep the diode, capacitor, and regulator-chip-lead lengths short.

The basic step-down configuration of **Fig 1** is relatively free of frequency-compensation difficulties. A simple RC damper network from the V_C pin to ground will usually suffice. Things become more complex when you add gain- and phase-contributing elements to the regulator's control loop. In these cases, you should view the regulator IC as a low-bandwidth power stage. The stage's delays arise from the sampled-data nature of its power delivery (100-kHz switching frequency) and its output LC filter. In general, limiting the regulator's gain-bandwidth product below that of the added loop elements will stabilize such a complex loop. This principle accords with established feedback theory.

Squeezing the utmost efficiency out of a switching regulator is a complex, demanding design task. Effi-

The most common magnetic-component problem is saturation.

ciency exceeding 80 to 85% requires some combination of finesse, witchcraft, and just plain luck. Interacting electrical and magnetic terms produce subtle effects that influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency isn't possible, but some guidelines do exist.

Losses fall into several loose categories including drive, junction, ohmic, switching, and magnetic. Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low-output-voltage switchers. For example, a 700-mV drop in a 5V-output switcher introduces more than a 10% loss. Though Schottky devices will cut the loss nearly in half, it is still appreciable. The ohmic losses in germanium diodes (now rarely used) are lower still, but switching losses negate the low dc drop of germa-

Techniques and equipment measure changing current

Accurately measuring rapidly changing current flow is essential to switching-regulator design. In many cases, current waveforms contain more valuable information than do voltage measurements.

The most powerful and convenient current-measuring tool is the clip-on current probe. The Tektronix P-6042 (bottom left in **Fig A**) is a Hall-effect, stabilized current transformer that responds from dc to 50 MHz.

These clip-on probes contain a current transformer and a Hall-effect transducer. The transducer senses current at dc and low frequencies; the transformer simultaneously processes the signal's high-frequency content. Their dc response allows you to determine the dc content of high-speed current waveforms. Sensitivities range from fractions of a milliampere to amperes.

The combination of convenience, broad bandwidth, and dc response make Hall-effect, stabilized current probes the instruments of choice for converter designers.

Transformer-based clip-on current probes are also available. Though they lack the dc response of their Hall-effect cousins, they're still quite useful. The Tektronix type 131 (upper left, **Fig A**), and the more modern 134, respond from hundreds of hertz to about 40 MHz.

AC current probes are also available with a simple termination (left foreground **Fig A**). These devices are more difficult to use than the actively terminated models because of their complex gain switching. Their low-frequency response is also poorer, although their high-frequency response exceeds 100 MHz.

The simple transformer (**Fig A**'s foreground) is a final form of ac current probe. These transformers are not clip-on devices, and they usually have significant performance limits compared with the clip-on instruments. However, they are inexpensive and can provide meaningful measurements when used according to manufacturers' recommendations. In practice, you thread the conductor through the opening provided and monitor the signal at the transformer's output pins.

Fig A also shows a wide-ranging dc clip-on current probe. The Hewlett-Packard 428B (upper right) responds from dc to only 400 Hz but features 3% accuracy over a 100-μA to 10A range. The instrument obviously cannot distinguish high-speed events, but it is invaluable for determining overall efficiency and quiescent current.

A great strength of these probes is that they take a fully floating measurement. Extract-

***Fig A—A host of devices can help** you make current measurements.*

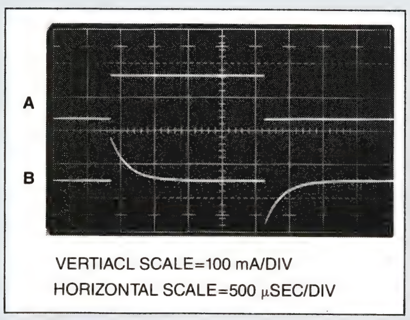


***Fig B—Trace A is the output of a** stabilized Hall-effect current probe, and trace B is the same signal measured with a transformer-based probe; clearly, the transformer-based probe is useless at low frequencies.*

nium at high switching speeds. In very low-power switchers, germanium's reverse leakage may be equally oppressive. Synchronously switched rectifiers are more complex, but can sometimes simulate a more efficient diode.

When evaluating rectifying and switching schemes, remember to include both ac and dc drive losses in your efficiency estimates. DC losses include base or gate current in addition to dc consumption in any driver stage. AC losses might include the effects of base or gate capacitance, transition-region dissipation (the switch spends some time in its linear region), and power lost because of timing skew between drive signals and actual switch action.

The LT1074 regulator IC's output switch, for example, comprises a PNP transistor driving a power NPN

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ing current information via magnetic coupling eliminates common-mode voltage considerations. As good as they are, however, current probes have limits and characteristics that you must remember in order to avoid unpleasant surprises. At high currents, for example, the probe may saturate. The saturation will corrupt the resulting CRT waveforms, rendering the measurement useless and confusing the unwary.

Further, for Hall-effect types, noise interferes with measurements below a few hundred microamperes. Luckily, this noise is obvious on the display.

Keep in mind that signal-transit delays vary from current probe to current probe and all are different from voltage probes. At high-sweep speeds these effects show up in multitrace displays as time skewing between individual channels. You can mentally factor in the current probes' transit-time delay to reduce error when interpreting the display. Note that active probes have the longest signal transit, on the order of 25 nsec.

Fig C—Current shunts are low-value resistors having 4-terminal connections for accurate current measurements.

When interpreting CRT displays,you must also keep in mind the low-frequency bandwidth restrictions of ac current probes. **Fig B** clearly demonstrates this principle by showing the ac probe's inability to follow low frequency. Similarly, remember that the probe's stated bandpass is −3 dB, meaning that signal information is not entirely present in the display at this frequency. When working at, or approaching, either end of the probe's bandpass consider that displayed information may be distorted or incomplete.

There are other ways to measure wideband current signals, although they're less convenient and desirable than clip-on current probes. Current shunts (**Fig C**, foreground) are low-value resistors with 4-terminal connections for accurate measurement. In theory, measuring voltage across a current shunt should yield accurate information. In practice, common-mode voltages introduce measurement difficulties, particularly at speed. Making such measurements requires an isolated probe or high-speed differential oscilloscope plug-in. The isolation amplifier in **Fig C** from Signal Acquisition Technologies (Minden, NV), has a 10-MHz bandwidth, a galvanically floating input, and 600V common-mode capability. The instrument allows any oscilloscope to take a floating measurement across a shunt.

Differential oscilloscope plug-ins, while not galvanically floating, can measure the voltage across a shunt. Tektronix types W, 1A5, and 7A13 have 1-mV sensitivity with a bandwidth as high as 100 MHz and excellent common-mode rejection. Types 1A7 and 7A22 have 10-μV sensitivity, although their bandwidth is limited to 1 MHz. All differential plug-ins have bandwidth or common-mode-voltage restrictions that vary with sensitivity. You must review these tradeoffs when you select the optimal shunt value for a particular measurement. In general, the smallest practical shunt value is preferable. This small value minimizes the inserted resistance's parasitic effects on the circuit's operation.

An empirical approach, using the ultimate simulator—a breadboard—is often the best way for you to select inductors.

transistor. The switch's drop can reach 2V at high currents. This drop will usually be the major loss in the circuit. You can mitigate the drop's effect on efficiency by using the highest possible input voltage. Higher output voltages will further minimize losses.

Actual losses from switch-saturation effects and diode drops are sometimes difficult to precisely ascertain. Changing duty cycles and time-varying currents make determining losses tricky. One simple way to judge relative losses is to measure various devices' temperature rises. Appropriate tools here include thermal probes and, at low voltages, the perhaps more readily available human finger. At lower power, even though the percentage of loss may be as great, the latter "digital" technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting changes in efficiency allows you to determine actual losses.

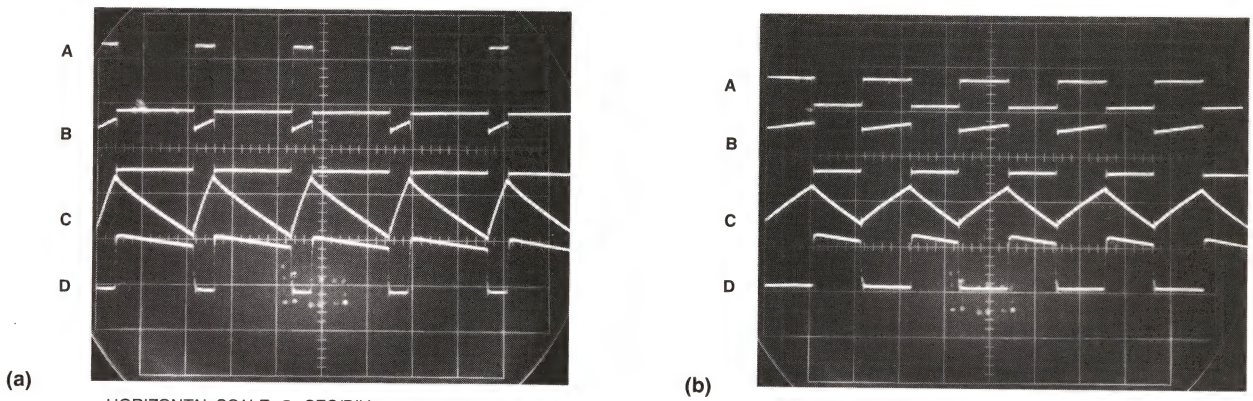
Ohmic losses in conductors are usually only significant at higher currents. Hidden ohmic losses include socket and connector-contact resistance and ESR in capacitors. ESR generally drops with capacitor value and rises with operating frequency. Consider the copper resistance of inductive components. You must often evaluate tradeoffs of an inductor's copper resistance versus its magnetic characteristics.

Switching losses occur when the switching device spends significant amounts of time in its linear region relative to operating frequency. At higher switching frequencies, transition times can engender substantial losses.

The design of the magnetic components also influences efficiency. Inductive-component design is well beyond the scope of this article, but some of the tradeoffs and specifications include core-material selection, wire type, winding techniques, size, operating frequency, current levels, temperature, and others. No substitute exists for access to a skilled magnetic-components specialist. Fortunately, the nonmagnetic losses previously mentioned usually dominate, allowing you to obtain good efficiencies with standard magnetic components. Thus, you usually need to employ custom magnetic components only after you have reduced other circuit losses to their lowest practical level.

Practical circuits

To illuminate practical circuits, first reconsider the simple example of a voltage step-down regulator in **Fig 1** with a 150-μH inductor installed. Conceptually, you can think of the regulator IC as having a switch between its V_{IN} and V_{SW} pins. When this "switch" closes, the input voltage appears at the inductor. Current flowing through the inductor-capacitor combination builds over time. When the switch opens, current flow



HORIZONTAL SCALE=5 μSEC/DIV

TRACE	VERTICAL
A	20V/DIV
B	1A/DIV
C	.2A/DIV (ON A 1A dc LEVEL)
D	1A/DIV

HORIZONTAL SCALE=5 μSEC/DIV

TRACE	VERTICAL
A	20V/DIV
B	1A/DIV
C	.2A/DIV (ON A 1A dc LEVEL)
D	1A/DIV

Fig 3—In these operating waveforms for Fig 1's *circuit with a 150-μH inductor installed and V_{IN}=28V, trace A is the V_{SW} pin's voltage and trace B is its current. Inductor current appears in trace C and diode current in trace D. The waveforms in **(a)** correspond to a 5V, 1-kΩ load while the waveforms in **(b)** show significant duty-cycle changes when the input voltage drops to 12V.*

ceases and the magnetic field around the inductor collapses.

As Faraday demonstrated, the voltage that the collapsing magnetic field induces is opposite in polarity to the originally applied voltage. As such, the inductor's left side becomes negative and the diode clamps it to ground. The capacitor's accumulated charge has no discharge path and a dc potential appears at the output; the dc potential is lower than the input voltage because the inductor limits current during the switch's on time. In this basic circuit, feedback-controlled switching action regulates the output voltage. Switch on time, and thus inductor charge time, vary to maintain the output-voltage level against changes in input voltage or output loading.

Ideally, no dissipative elements exist in this voltage step-down conversion. Thus, although the output voltage is lower than the input voltage, no energy-conversion losses occur. In practice, the circuit elements *do* have losses, of course, but step-down regulator efficiency is still higher than with inherently dissipative, voltage-divider approaches.

Components at the regulator IC's V_C compensation pin control the IC's frequency compensation, stabilizing the feedback loop. You select the feedback resistors to force the voltage at the FB feedback pin to match the device's internal 2.5V reference value.

Fig 3a shows operating waveforms for the regulator at $V_{IN}=28V$ with a 5V, 1-kΩ load. Trace A is the V_{SW} pin's voltage; trace B is its current. Inductor current appears in trace C; diode current appears in trace D. Examining the current waveforms allows you to determine the V_{SW}'s and diode path's contributions to the inductor's current. Note that the inductor current's waveform occurs on top of a 1A dc level. **Fig 3b** shows significant duty-cycle changes when V_{IN} drops to 12V. This lower input voltage requires longer inductor-charge times to maintain the required output level.

Dual-output step-down regulator

Fig 4, a logical extension of the basic step-down switching regulator, provides positive and negative outputs. The circuit is essentially identical to **Fig 1's** basic switcher, except that it has a winding coupled to L_1. This floating winding's output gets rectified, filtered, and regulated to a $-5V$ output. The negative output can use a positive voltage regulator because its floating bias allows you to assign the regulator's output terminal to ground. You can also reference its output to any voltage within the breakdown capability of the device. Hence, the secondary output *could* be $+5V$ or, if stacked on the $+15V$ output, $+20V$.

Flux pickup from L_1's driven winding sets the limit for negative output power. With a 2A load at the $+15V$ output, the $-5V$ output can supply more than 500 mA.

You can also obtain negative outputs with a simple,

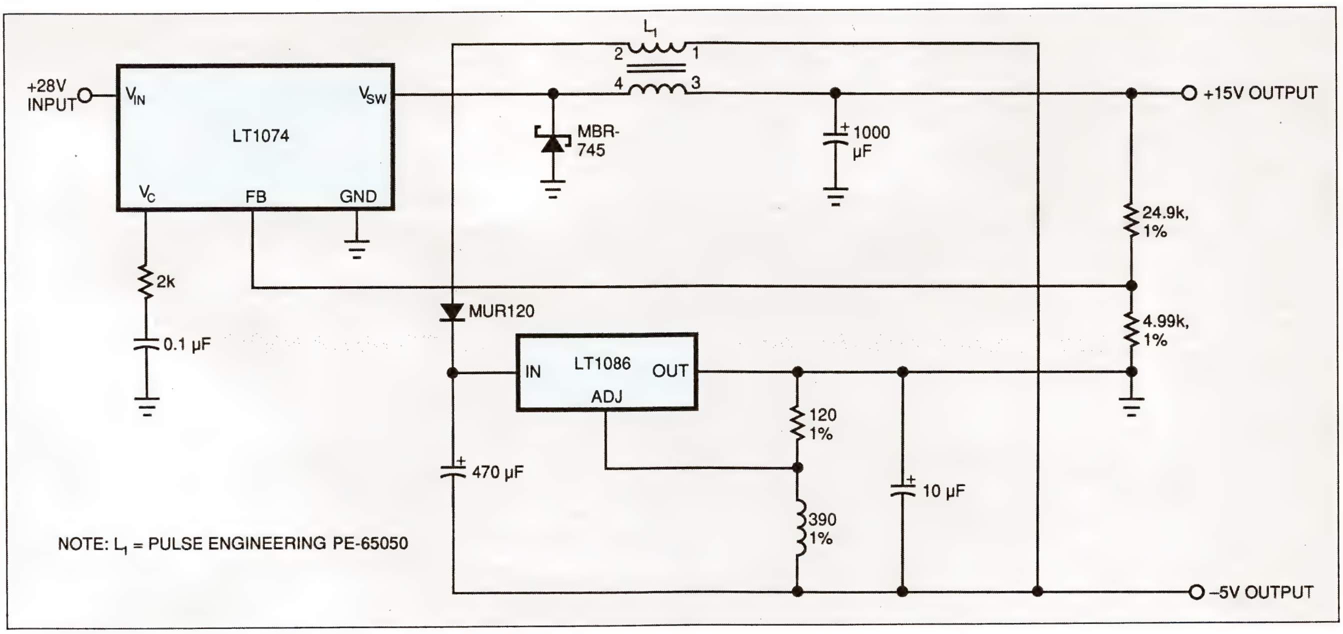


Fig 4—Adding a coupled winding to the basic circuit's inductor allows you to tap off a floating auxiliary output.

Confronting the challenge of selecting the proper inductor, engineers often simply insert an anonymous drawer dweller into an unsuspecting circuit.

2-terminal inductor instead of a multiwinding inductor **(Fig 5)**. You essentially ground the inductor and steer the catch diode's negative current to the output. IC_2 closes the loop by inverting and scaling the negative output to the regulator IC's feedback pin. The 1% resistors' scale factor sets output voltage; the RC network around IC_2 gives frequency compensation. Waveforms for this circuit are reminiscent of **Fig 1**'s, with the exception that diode current is negative.

Fig 6, which we call "Nelson's circuit," provides the same function as the previous circuit, but eliminates the level-shifting op amp. Circuit ground is common to input and output. Connecting the regulator IC's ground pin to the negative output accomplishes the design's level shift. The regulator IC senses feedback relative to the circuit's ground, and it drives its output so as to force its feedback pin to be 2.5V above its ground pin. The previous negative-output circuit has

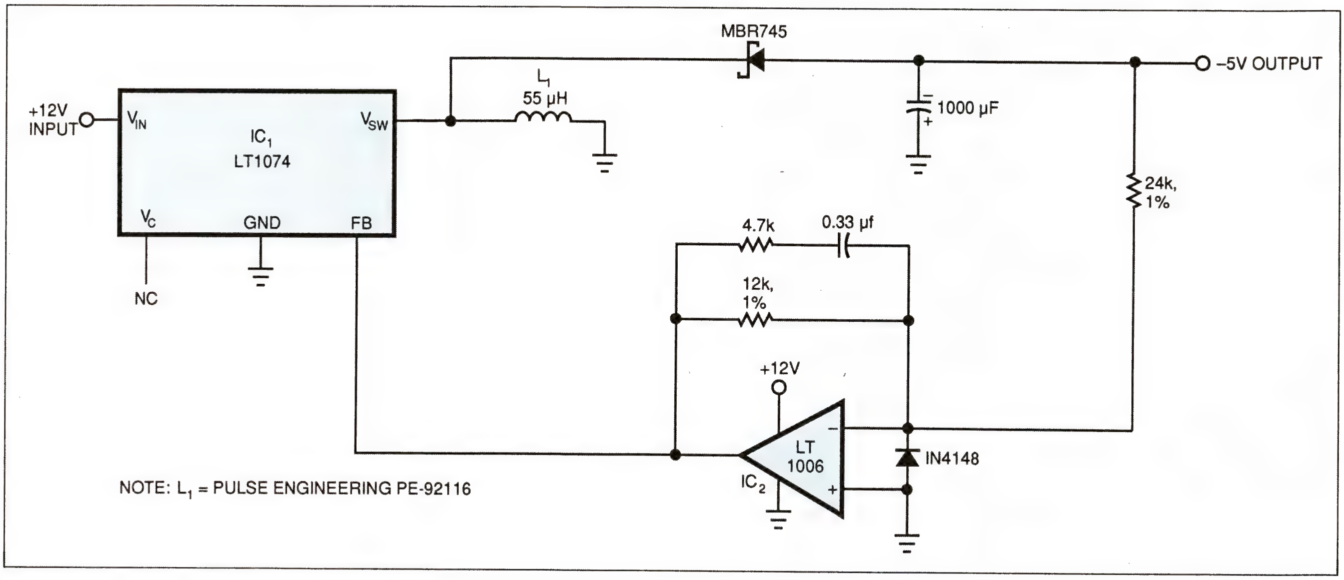


***Fig 5—You can obtain negative outputs** using a simple 2-terminal inductor—if you ground one end and properly orient the catch diode.*

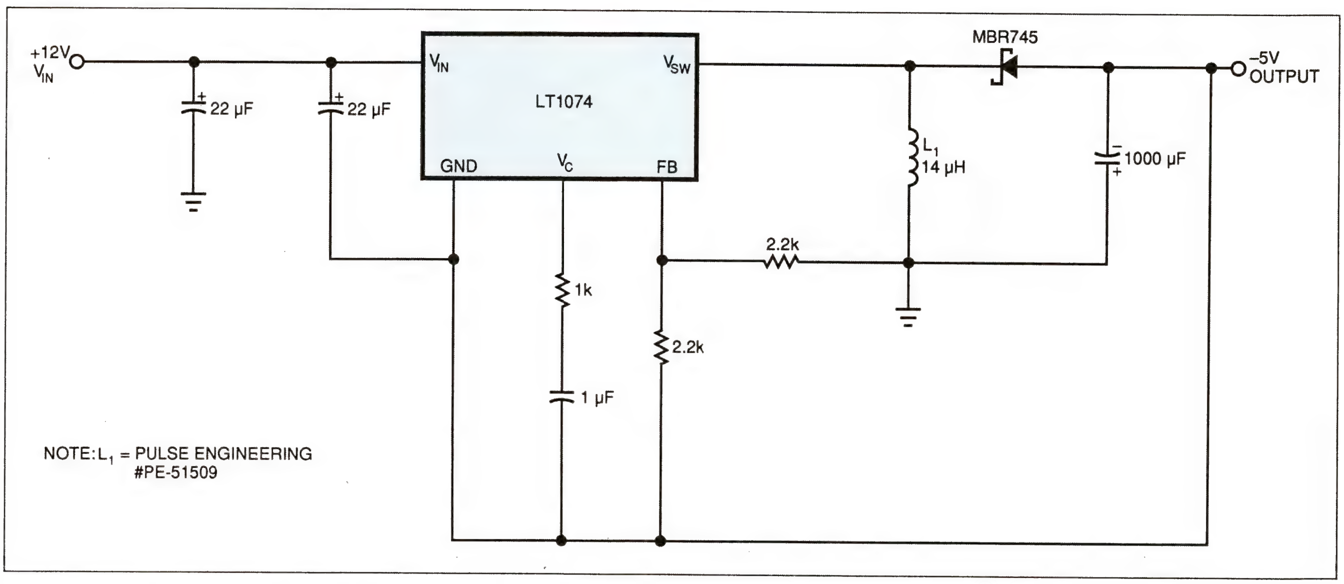


***Fig 6—This negative-output circuit** eliminates the level-shifting op amp. Connecting the regulator IC's ground pin to the negative output accomplishes this design's level shift.*

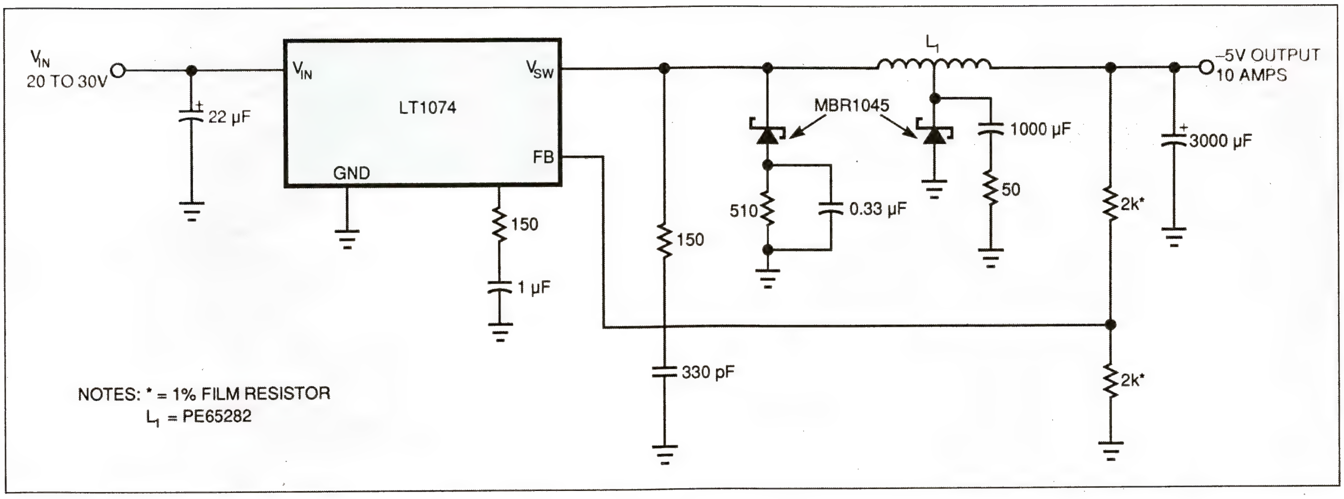


Fig 7—Don't be fooled. D_1 is not a catch diode; it's part of a snubber circuit. *D_2 is the catch diode. When D_2 conducts, it switches out a portion of the inductor's turns, forcing the inductor's magnetic field to deliver its stored energy through an effectively smaller inductance and thereby increasing the circuit's output-current capability.*

two advantages, compared with Nelson's. First, the package can directly contact a grounded heat sink. Second, the IC's control pins are ground referred.

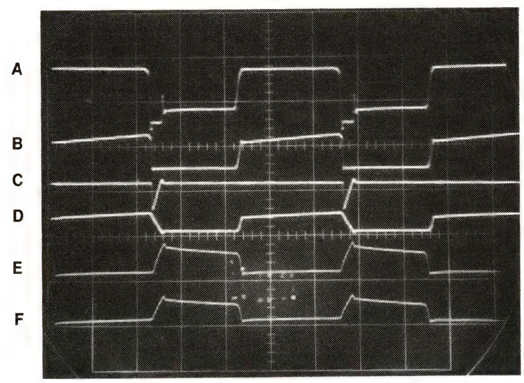
Note that the inductor values in both negative-output designs are notably lower than in the positive-output designs. The reduced loop-phase margin of these circuits demands the lower-value inductors. Higher inductance values, while preferable for limiting peak current, will make the loop unstable or even cause it to oscillate.

Current-boosted step-down regulator

Fig 7 shows a novel way to obtain significantly higher output currents—by utilizing efficient energy storage in the regulator IC's output inductor. The technique prolongs current flow from the inductor and thereby effectively increases the inductor's duty cycle, compared with the standard step-down switching regulator's, allowing more energy storage in the inductor. But beware, the increased output current comes at the cost of higher output-voltage ripple.

The key to the design is its tapped inductor. With it, the circuit has current gain. If N is the ratio of switch-side turns to output-side turns, current delivered to the output will be N+1 times higher during the V_{SW}'s off time as compared to the current flowing during its on time.

Fig 8 shows the circuit's operating waveforms. Its operating characteristics are initially similar to that of the step-down switching regulator in **Fig 1**. During V_{SW}'s on time (trace A), the regulator IC applies the input voltage to one end of the tapped inductor. Because inductor current (trace F) is still present, current from the V_{SW} pin (trace B) ramps up almost instantaneously, then slows as the core stores energy. The current proceeds into the inductor (trace D) and finally to the load.



HORIZONTAL SCALE=2 µSEC/DIV

TRACE	VERTICAL
A	50V/DIV
B	5A/DIV
C	10A/DIV
D	10A/DIV
E	10A/DIV
F	10A/DIV

Fig 8—In these operating waveforms for Fig 12's *circuit, trace A is V_{SW}'s voltage, trace B is its output current, trace C is the snubber circuit's D_1 current, trace D is the inductor's input current (minus the snubber circuit's contribution), trace E is the current through D_2, and trace F is the output current.*

Think carefully about your capacitors' requirements; you must account for all operating conditions.

When the V_{SW} pin is off, current is no longer available to charge the inductor. The magnetic field therefore collapses, causing the V_{SW} pin's voltage to go negative, ending the similarity to the basic regulator. In the modified version the output current (trace F) receives a boost as the magnetic field collapses. The boost results when the energy stored in the tapped inductor transfers to the output. This current step circulates through C1 and D2 (trace E) and increases the output-voltage ripple.

Not all the energy, however, transfers to the output-side turns. Current (trace C) will continue to flow in the switch-side winding because of leakage inductance, whose effects are suppressed by a snubber network. To minimize snubber losses, the tapped inductor is bifilar wound for maximum coupling.

In most instances the switching regulator's output will go directly to the load. However, those applications requiring faster transient response or reduced noise will benefit from linear post regulation. To incur minimal efficiency losses, you must set the switching-regulator IC's output to provide just enough voltage to the linear regulator to maintain regulation. In such applications, a low-dropout linear regulator works best.

Post regulation, variable case

Some applications require variable linear post regulation (**Fig 9a**). The circuit operates with little efficiency sacrifice. The linear regulator operates in normal fashion, supplying a variable 1.2 to 28V output. The remainder of the circuit forms a switched-mode preregulator that maintains a small, fixed voltage

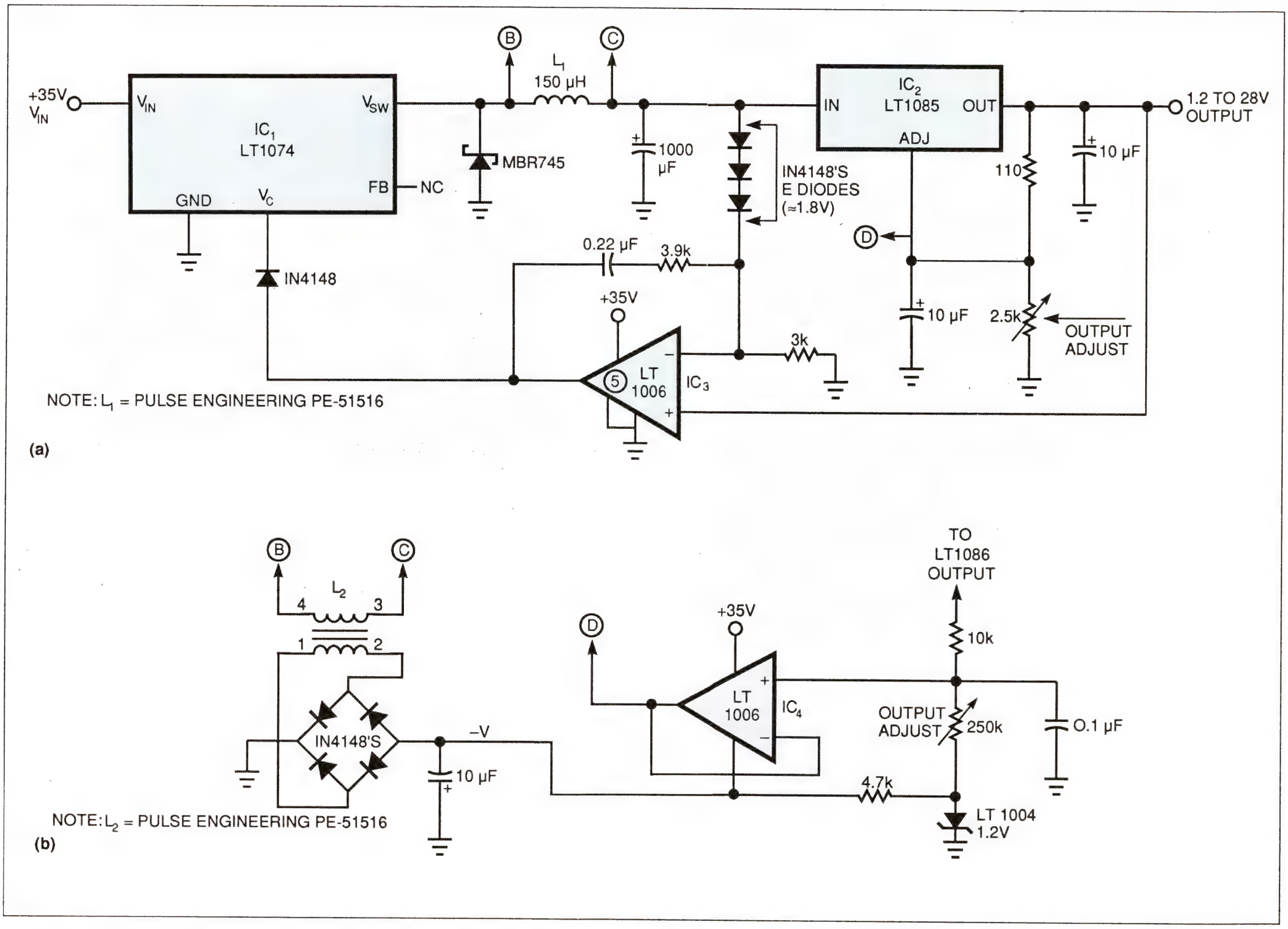


Fig 9—The feedback loop of this variable-output regulator, (a), *ensures that the voltage impressed across the linear postregulator, set by the "E" diode string, is always just the minimum voltage it needs to operate. The optional circuit in* ***(b)*** *permits output voltages down to 0V.*

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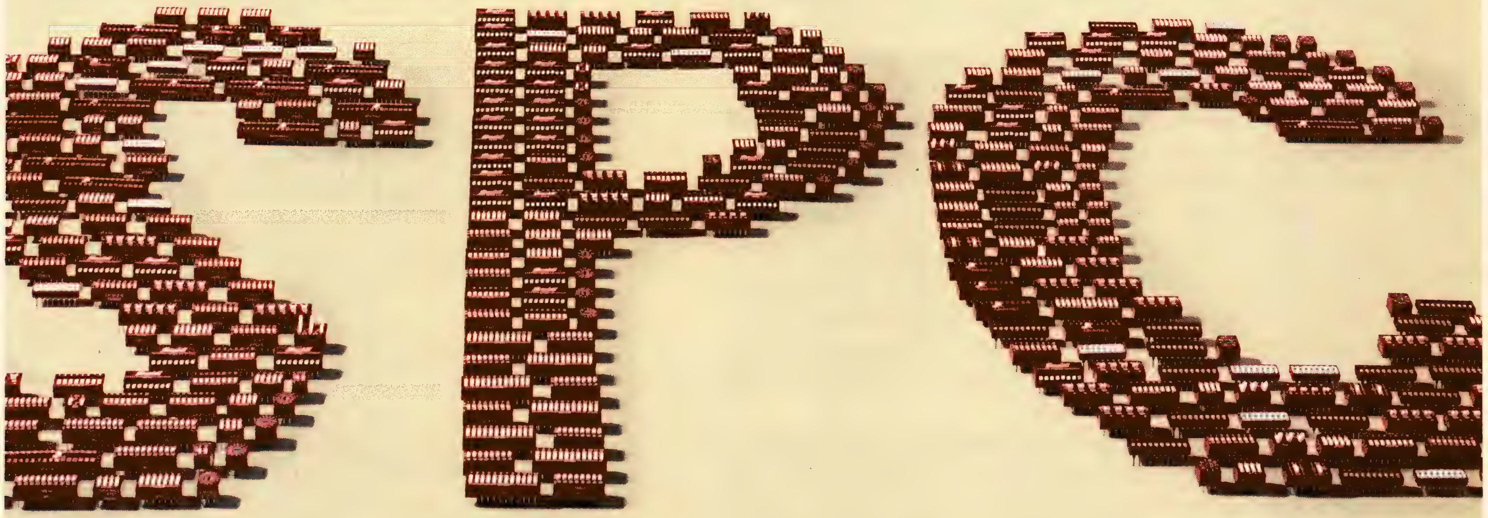

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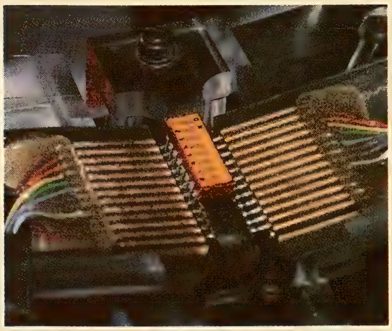

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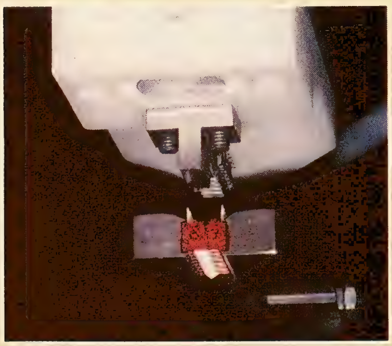

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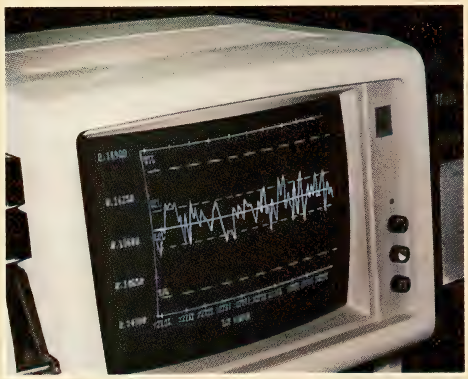

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Layout is vital; don't mix signal, frequency-compensation, and feedback returns with high-current returns.

across the linear regulator regardless of its output.

IC_3 biases the step-down switching regulator to produce whatever voltage is necessary to maintain the "E diodes" potential across the linear regulator. You can adjust the number of diodes in the "E diode" string to achieve different voltages across the linear regulator. IC_3's inputs are balanced when the linear regulator's output is "E diodes" below its input. IC_3 maintains this condition regardless of line, load, or output-voltage conditions. Thus, the circuit maintains good efficiency over the full range of output voltages. The RC network at IC_3 compensates the loop.

Deliberately introducing a positive offset to IC_3 ensures loop startup. Grounding IC_3's appropriate balance (in this case pin 5), induces the offset, resulting in a positive 6-mV offset, which, normally considered poor practice because it increases amplifier drift, causes no measurable error in this application. As shown, the circuit cannot produce outputs below the regulator IC's 1.2V internal reference. Applications requiring outputs adjustable down to 0V will benefit from the option in **Fig 9b**, which replaces L_1 with L_2. L_2's primary winding performs the same function as L_1's, while its coupled secondary winding produces a negative-bias output, $-V$. The negative bias allows regulated outputs down to 0V.

The $-V$ potential derived from L_2's secondary winding varies considerably with operating conditions; wildly varying duty cycles necessitate the optional circuit's full-wave bridge rectifier. The high feedback string values and IC_4's buffering ensure that the circuit will be stable for "starved" values of $-V$. IC_4 and its attendant circuitry replace all components associated with the linear regulator's ADJ pin.

Low quiescent-current regulators

Many applications require currents in the ampere range under normal conditions, but only microamperes while in standby or "sleep" mode. A typical laptop computer, for example, may draw 1 to 2A running, but need only a few hundred microamperes for its memory when turned off. In theory, any regulator, with a loop properly designed to be stable under no load, will work. In practice, a switcher having relatively large quiescent current may be unacceptable because of excessive battery drain during low current-output periods—even if it operates serenely.

Fig 10's simple loop effectively reduces circuit quiescent current from 6 mA to only 250 μA. The circuit uses the regulator IC's shutdown pin. When the circuit

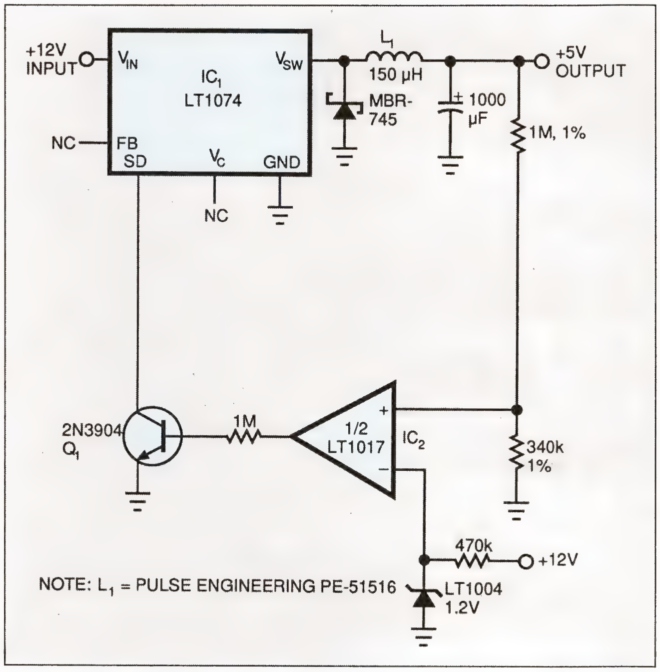

*Fig 10—**This circuit's simple loop** reduces its quiescent current from 6 to only 250 mA by switching the regulator off at low loadings.*

pulls this pin to within 350 mV of ground, the IC shuts down and draws only 1200 μA. Short on times keep the duty cycle low, resulting in the small, effective quiescent current. Comparator IC_2 combines with the regulator IC's reference and Q_1 to form a "bang-bang" control loop around the regulator IC, which bypasses the regulator IC's internal feedback amplifier and reference.

When the circuit's output falls slightly below 5V, IC_2's output switches low, turning off Q_1 and enabling the regulator IC. The V_{SW} pin then pulses at full duty cycle, forcing the output back above 5V. IC_2 then biases Q_1 on again, the regulator IC goes into shutdown, and the external loop's action repeats. The frequency of this on-off control action is directly load dependent, with typical repetition rates of 0.2 Hz at no load. The on-off operation combines with the LC filtering action in the regulator's V_{SW} line to generate an output hysteresis of about 50 mV.

The external loop performs well but has two potential drawbacks. At higher output currents the loop oscillates in the 1 to 10-kHz range, causing audible noise, which users may object to. Also, the control loop's operation forces about 50 mV of ripple on the output. Ripple frequency ranges from 0.2 Hz to 10 kHz depending on input voltage and output current.

Transients usually cause the most trouble for diodes, introducing stresses whose results are often hard to predict.

Fig 11's more sophisticated circuit eliminates these two problems with some increase in complexity while maintaining quiescent current at 150 μA. The technique is particularly significant, having broad implications in battery-powered systems because you can easily apply it to a wide variety of regulators.

Fig 11's signal flow is similar to **Fig 10**'s, but additional circuitry appears between the feedback divider and the regulator IC. The circuit does not use the regulator IC's internal feedback amplifier and voltage reference. Under no load, the output voltage will slowly ramp down over a period of seconds, during which the comparator IC_1's output is low, as are the outputs of the paralleled 74C04 inverters. The inverters, in turn, pull the regulator IC's V_C pin low, forcing the IC to a zero duty cycle. Simultaneously, IC_2's output is low, putting the regulator in shutdown mode. Therefore, the V_{SW} pin is off and no inductor current flows.

When the output drops by about 60 mV, IC_1 triggers and the inverters go high, pulling the V_C pin up and biasing the regulator. IC_2 also rises, taking the IC out of shutdown mode. The V_{SW} pin then pulses the inductor at its normal, 100-kHz clock rate, causing the output to rise abruptly. This action trips IC_1 low, forcing the V_C pin back low and shutting off V_{SW}'s pulsing. IC_2 also goes low, putting the IC back into shutdown.

This "bang-bang" control loop keeps the 5V output's level within the loop's 60-mV hysteresis window. Note that compared with the loop's oscillation period of seconds, the R_1-C_2 time constant at V_C is not significant. Because the regulator spends almost all of its time in shutdown mode, the circuit draws very little quiescent current—150 μA.

As the load increases, the loop's oscillation frequency increases to keep up with the load's demand; R_1-C_1 begins to filter the waveform at the V_C pin. If the load continues to increase, the loop's oscillation frequency will also increase. The R_1-C_1 time constant, however, is fixed. Beyond some frequency, R_1-C_1 must average loop oscillations to dc. Here, the V_C waveform becomes heavily filtered at loads of 7 mA and above. At 1A

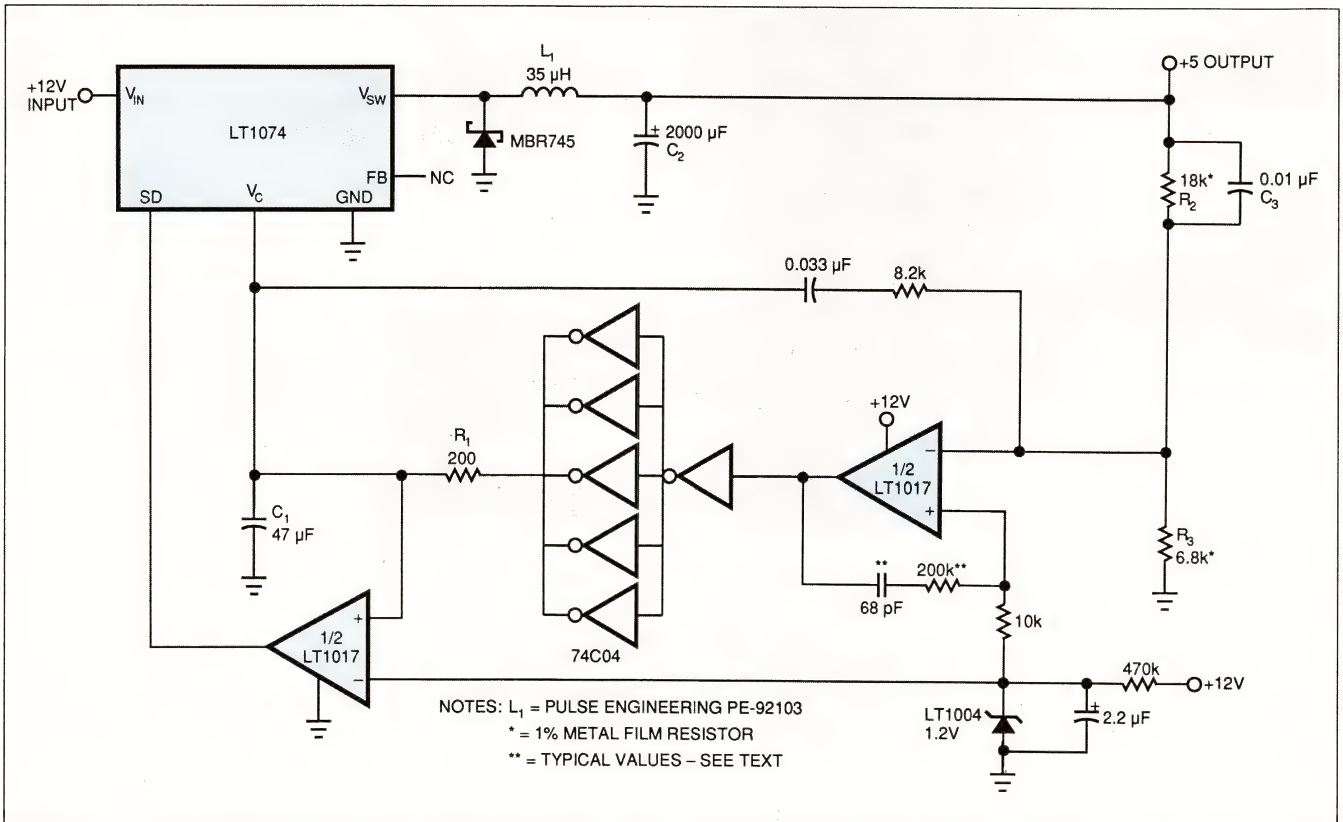

***Fig 11—The RC filter at the regulator IC's** V_C pin gradually filters the quiescent-current, switched-feedback circuit's pulsed output to a steady dc signal as the output load increases, thereby canceling unwanted cycling of the regulator IC at high loads.*

In theory, any regulator, with a loop properly designed to be stable under no load, will work.

loads, the regulator IC's V_C pin will see pure dc; the regulator IC will be running at its full 100-kHz clock rate.

With the V_C pin at dc, you can conveniently think of IC_1 and the inverters as a linear error amplifier with a closed-loop gain set by the R_2-R_3 feedback divider. In fact, IC_1 is *still* trying to modulate the duty cycle at the V_C pin, but at a rate far above R_1-C_1's break frequency. R_1-C_1's roll-off and the phase lead of C_3 into IC_1 dominate C_2's phase error (C_2 was, after all, selected for low loop frequency at low output currents).

The loop is stable and responds linearly for all loads beyond 10 mA. In its high-current region, the regulator IC is desirably fooled into behaving like a conventional step-down regulator.

Formal analysis difficult

A formal stability analysis for this circuit is quite complex; simplifying it somewhat lends insight into the loop's operation. At 250 μA, C_2 and the 20-kΩ load form a decay-time constant exceeding 30 sec. This delay is orders of magnitude larger than R_2-C_2, R_1-C_1, or the regulator IC's 100-kHz commutation rate. As a result, C_2 dominates the loop. Wideband comparator IC_1 sees phase-shifted feedback, and very low-frequency oscillations occur. Although C_2's *decay* time constant is long, its *charge* time constant is short because the circuit has low sourcing impedance. This difference accounts for the ramp nature of the oscillations.

Increased loading reduces the C_2-load decay time constant. As loading increases, the loop oscillates at a higher frequency because of C_2's decreased decay time. When the load impedance becomes low enough, C_2's decay time constant ceases to dominate the loop. R_1 and IC_2 almost entirely determine this point. Once R_1 and IC_2 reign as the dominant time constant, the loop begins to behave like a linear system. Now, C_3 becomes significant, performing as a simple feedback lead to smooth output response ("zero compensation" for all you technosnobs out there).

A fundamental tradeoff exists for C_3's phase lead. When the switcher is running in its linear region, C_3's phase lead must dominate the loop's time-lag-generated hysteretic characteristic. As such, select C_3 to be the best compromise between output ripple at high load and loop-transient response.

Despite the circuit's complex dynamics, its transient response is quite good. Further, its high-power efficiency is similar to standard switchers; low-power efficiency is somewhat better—although poor in the lowest ranges. The poor efficiency is not particularly bothersome, because power loss is very small.

The loop provides a controlled, conditional instability instead of the usually more desirable (and often elusive) unconditional stability. This deliberately introduced instability dramatically lowers switcher quiescent current without sacrificing high-power performance. EDN

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

Article Interest Quotient (Circle One)
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Now that we've been properly introduced,

Intel To Show 2-Mb, 4-Mb EPROMs

By David Roman

TOKYO — Intel Corp. chairman Gordon Moore will introduce his company's highest-density EPROMs at a press conference here tomorrow.

Intel executives are flying to Tokyo to take the wraps off two 2-megabit EPROMs and one 4-Mbit EPROM to demonstrate the company's commitment to the Japanese market.

Though Intel is the world's leading producer of EPROMs, the company owns less than 5% of Japan's EPROM market, said Tom Price, marketing manager of Intel's Programmable Memory Operation.

Intel owned 18% of the world's $1.8 billion EPROM market in 1988, according to Dataquest Inc.

The Japanese market has been quick to pick up high-density EPROMs, Price said, and Intel is hoping t- some market -- its 128- which is

× 8 (2-Mbit) part; and a 4-Mbit EPROM organized as 256-K × 16, which will be in production in August.

Moore said these chips could reduce the number of memory chips in a system up to 75% while facilitating the design of more-compact systems.

Fujitsu Ltd., NEC Corp. and Toshiba Corp. are the only manufacturers shipping either 2- or 4-Mbit EPROMs, according to Dataquest industry analyst Mary Olsson.

Though Japanese suppliers made their public announcements of 2- and 4-Mbit EPROMs before Intel did, Price said Intel is determined to ramp very quickly to volume production.

Intel's swift ramp-up of its 2- and 4-Mbit EPROMs will bring selling prices down quickly; in terms of cost per bi- parts will -

Intel's Moore: In Japan to show off his company's densest EPROMs.

The Intel parts are all produced with the same 1-micron CHMOS process Intel uses to build - 80386 microprocess- -pany plans to - 1.2-micro- -oductio-

ration costs $55 apiece; the 25- K × 8 configuration costs - apiece in 10,000-piece qu- ties. Faster, 150-ns vers- all the new EPROMs w- for about 25% more.

The byte-wide (256- part comes in a 32-p- while the 16-bit- come in 40-pin c- 32-pin and 40-pin the same ones - Mbit EPROM word widths future EPR density. Intel surf- M-

Intel erweitert EPROM-Spektrum nach oben

2- und 4-Mbit-EPROMs in 1,0-µm-CMOS-Technologie

002 **Ein 4-Megabit-EPROM und zwei Architektur-Varianten des 2-Megabit-Typs hat Intel vorgestellt. Die neuen Speicherbauelemente werden in 1-µm-CHMOS-III-E Technologie gefertigt und haben Zugriffszeiten zwischen 150 und 200 ns. Die bereits in Mustern verfügbaren Bausteine, deren Massenproduktion im August anläuft, sind auch im PLCC-Gehäuse erhältlich.**

Das EPROM 27C240 ist ein nichtflüchtiger Speicher mit einer Kapazität von 4 Mbit, organisiert zu 256K × 16 bit, und mit 150 oder 200 ns Zugriffszeit verfügbar. Es hat ein 40poliges Keramik-DIL-Gehäuse nach Jedec-Standard und ist aufwärtskompatibel zu Intels 1-Megabit-EPROM 27C210 im 40poligen DIP. Um den unterschiedlichen Systemauslegungen und Prozessorbuserfordernissen entgegenzukommen, bietet Intel auf der 2-Megabit-Ebene zwei Architekturen an. Das EPROM 27C220 ist zu 128K × 16 bit organisiert und bietet mit seinem 40poligen Keramik-DIP ebenfalls eine direkte Nachrüstmöglichkeit vom 1-Mbit-Typ 27C210. Diese Architektur ermöglicht den wirtschaftlichsten und kompaktesten Platinenentwurf für Systeme wie etwa Personalcomputer, die lediglich ein oder zwei EPROMs zum Speichern von Boot-Code oder BIOS Software benötigen.

Das 2-Mbit-EPROM 27C020 organisiert zu 256K × 8 bit und untergebracht im 32poliger DIP, eignet sich optimal für leistungsstarke Mikroprozessor-Schaltungen mit zahlreichen, in Speicherbänken angeordneten EPROMs, die komplexe Datengramme oder grosse Datenmengen speichern. Typische

NEWS
JAPAN

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きたと思う。ただ、多
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間がかかる。顧客の姿勢も変
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さて、今回発表された
ROMだが、アクセスタイム
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ビット構成の27C240
は従来の1Mビット
210EPROMのアッ
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K×16ビッ
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BIOSソフトをストアするパソコンのようなシステムに適したメモリだ。

もう1種類の2M EPROM(256K×8)27C020は、高性能組み込み制御システムなどに最適。たとえばページプリンタのように、複雑なプログラムや大量のコード記憶に多数のEPROMを使用するシステムでの利用が考えられる。いずれもサンプル出荷は始まっているが、量産に入るのは今年9月から。

インテルでは今後、メモリビジネスとしてEPROMとフ
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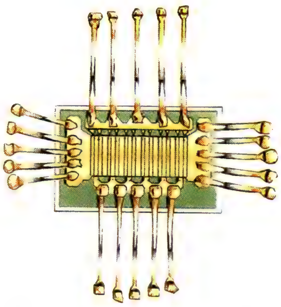

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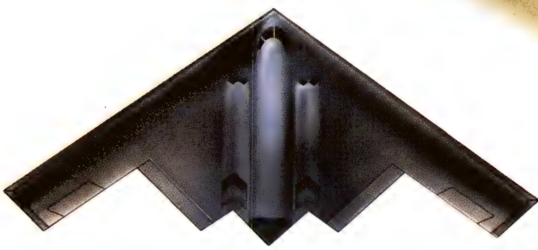

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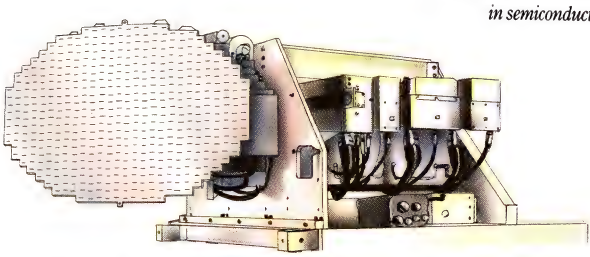

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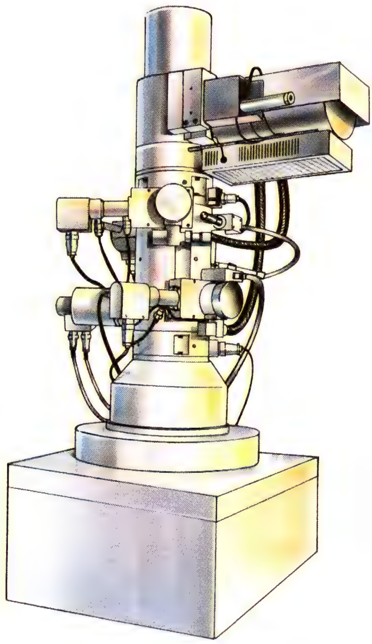

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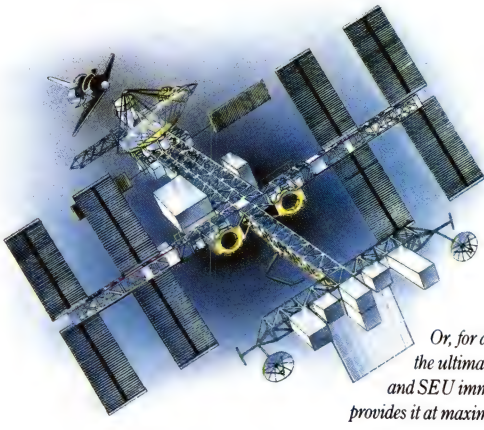

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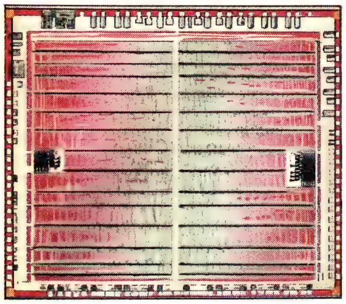

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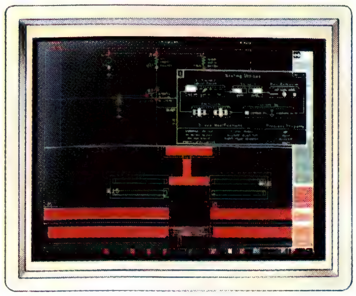

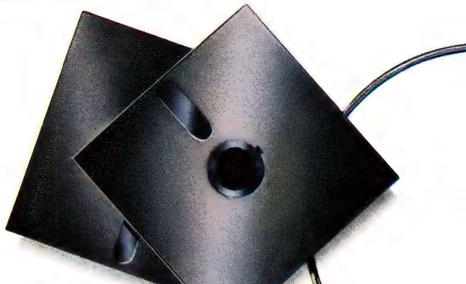

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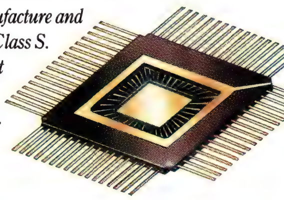

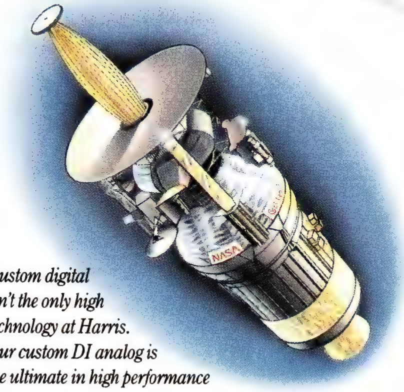

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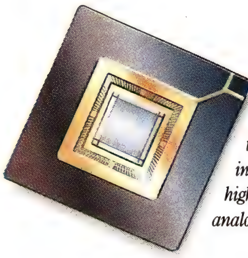

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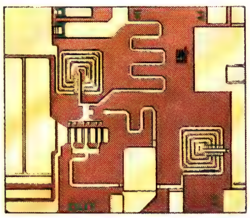

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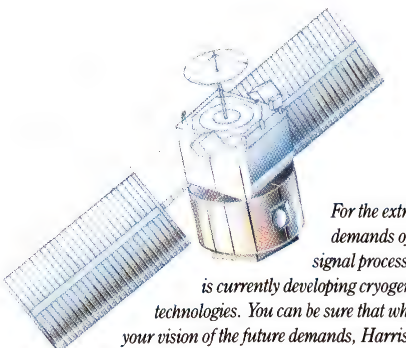

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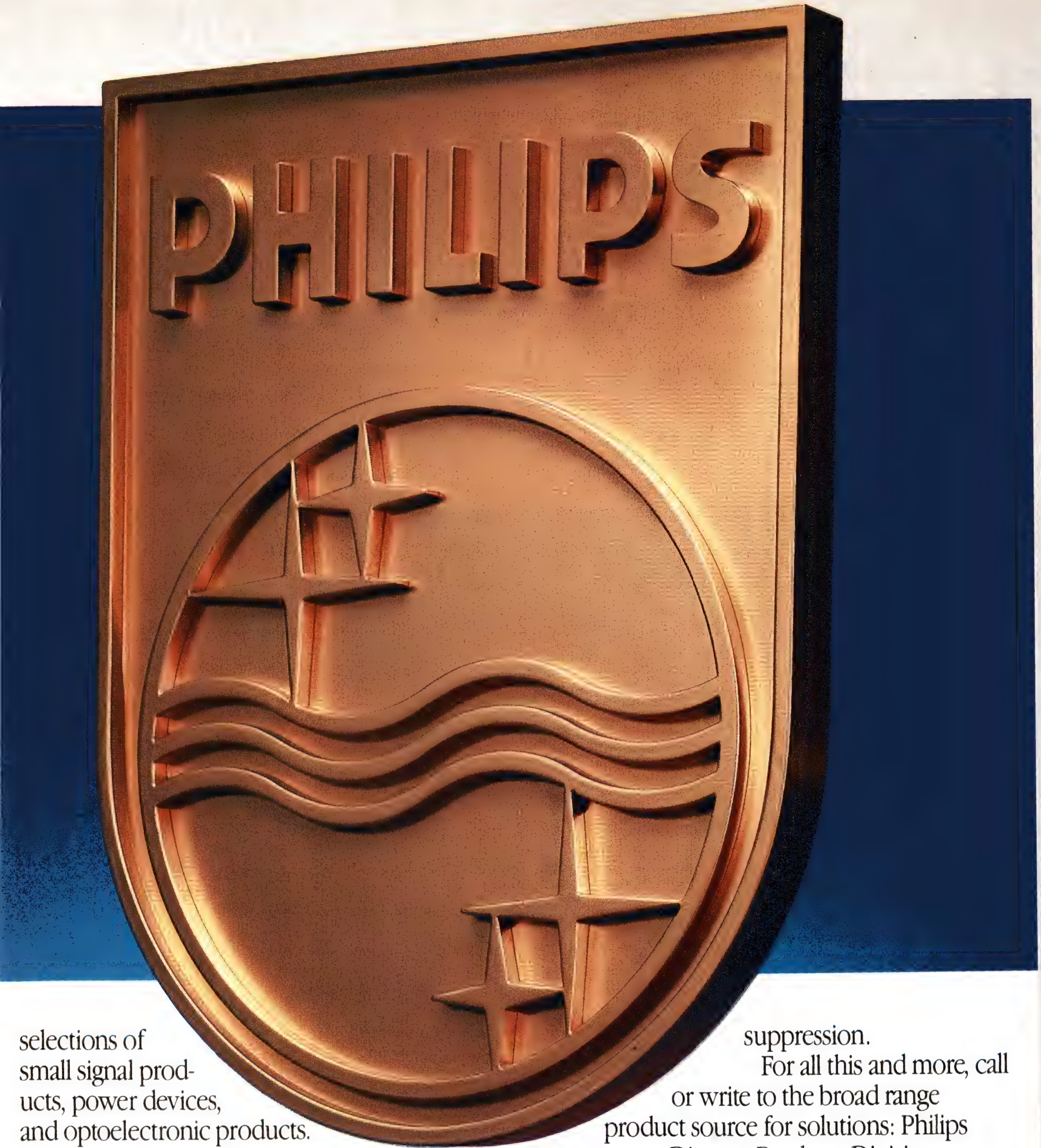

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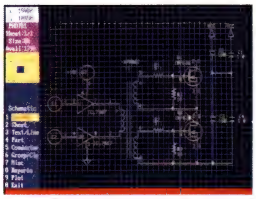

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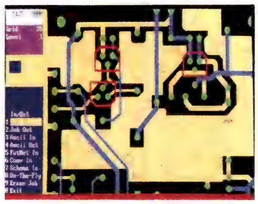

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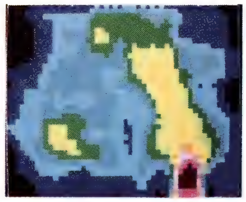

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EDITED BY CHARLES H SMALL

Program plots transformer response

Hugh M Adams, PE
Rtronics Inc, Pensacola, FL

The HP Basic program in **Listing 1** plots the leading edge of the step response of a high-voltage transformer after you input all of its known, or measurable, parameters. **Fig 1** shows a high-voltage transformer's equivalent circuit with all elements referred to the secondary side. This program helps you quickly evaluate the effects that the many different, specialized winding techniques employed in high-voltage transformers will have on your design.

To Vote For This Design, Circle No. 746

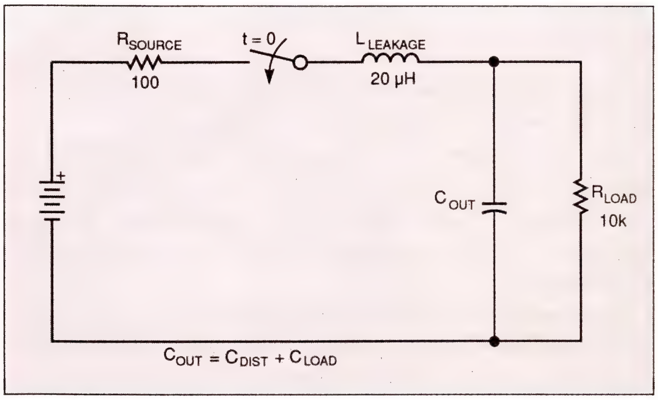


***Fig 1—This simple model,** embodied in the program in **Listing 1**, incorporates the known and measurable parameters of a high-voltage transformer.*

Listing 1—HP Basic, high-voltage-transformer step-response program

```
10 GCLEAR
20 CLEAR
30 DISP "PLOT OF STEP RESPONSE OF HV TRANSFORMER"
40 DISP "ENTER R1,R2,L(UH),C(PF)";
50 INPUT R1,R2,L,C
60 L=L*.000001 @ C=C*.000000000001
70 D=(C*R1+L/R2)*(L*C)^-.5*(1+R1/R2)^-1.5
80 D=D/2 @ D=INT (1000*D)/1000
90 DISP "DELTA =";D
100 RAD
110 P=0
120 W1=(L*C)^-.5*(1+R1/R2)^-.5
130 DISP "RING FREQUENCY=";INT (W1/2*PI );" HZ"
140 DISP @ DISP @ DISP @ DISP "PRESS 'CONT' TO SEE PLOT"
150 PAUSE
160 LOCATE 25,150,25,80
170 SCALE 0,.00001,0,2
180 FXD 1,1
190 LAXES .000001,.5,0,0,1,.5
200 FOR T=0 TO .00001 STEP .00000005
210 V=(1+(1-D^2)^-.5*EXP (-(D*W1*T))*SIN (W1*(1-D^2)^.5*T-P))*(R2/(R1+R2))
220 PLOT T,V
230 NEXT T
240 MOVE .0000005,2.3
250 LABEL "R1/R2=";R1/R2;"R1=";R1;"L/C=";L/C;"C=";C*1.E12;"PF"
260 MOVE .0000005,2.1
270 LABEL "DELTA=";D;"FREQ=";INT (W1/2*PI );" HZ"
280 MOVE .000004,-.85
290 LABEL "TIME"
300 END
```

PLD expands arbiter chip

Ted Burton and Charlie Dike
Signetics, Orem, UT

If you expand the 74F786 high-speed, 4-input bus arbiter using the chip's built-in, independent, 4-input AND gate **(Fig 1a)**, the resulting solution will be seriously flawed. Any activity on bus-request lines A through D can block bus requests on lines E through G. The circuit in **Fig 1b** overcomes this deficiency.

You can generalize **Fig 1b**'s scheme to accommodate any number of inputs if your expanded circuit follows two rules. First, any two bus-request lines must connect to at least one arbiter chip. Second, the PLD must assert the proper bus-grant line for any possible combination of valid inputs from the arbiter chips.

The PLD must recognize two possible classes of valid inputs. Obviously, if a given input to the arbiter chips wins *all* of its arbitration contests taking place in all the chips to which it's applied, the PLD must grant that input's bus request (the $\overline{A_1A_2}$ term in **Listing 1** for $\overline{BG_A}$'s equation, for example). In addition, you must program the PLD to grant only one bus request arbitrarily when two or more bus-request lines win some—but not all—of their respective arbitration contests (for example, the remaining minterms in the $\overline{BG_A}$ equation). EDN

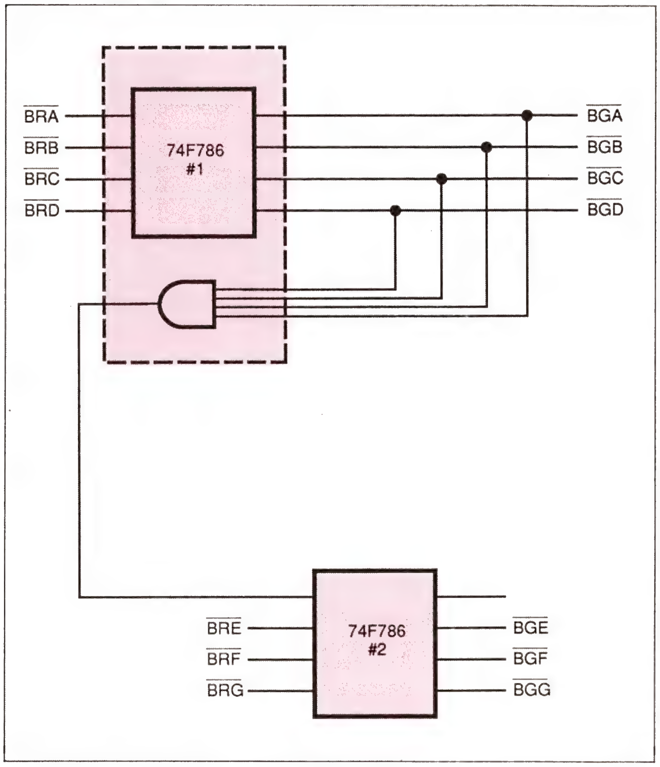


Fig 1a—Using the 74F789's built-in AND gate to expand the number of bus-request lines beyond four isn't a perfect solution.

To Vote For This Design, Circle No. 747

Listing 1—Arbitration-PLD equations

$\overline{BGA} = \overline{A1A2} + \overline{A1B2} + \overline{C1A2E3} + \overline{C1A2F3}$
$\overline{BGB} =$
$\overline{B1B2} + \overline{B1A2} + \overline{C1B2E3} + \overline{C1B2F3} + \overline{D1B2E3} + D1B2F3$
$\overline{BGC} = \overline{C1C3} + \overline{C1D3} + \overline{B1E2C3} + \overline{B1F2C3}$
$\overline{BGD} =$
$\overline{D1D3} + \overline{D1C3} + \overline{D1A2E3} + \overline{D1A2F3} + \overline{B1E2D3} + \overline{B1F2D3}$
$\overline{BGE} = \overline{E2E3} + \overline{E2F3} + \overline{A1E2C3} + \overline{A1E2D3}$
$\overline{BGF} = \overline{F2F3} + \overline{F2E3} + \overline{A1F2C3} + \overline{A1F2D3}$

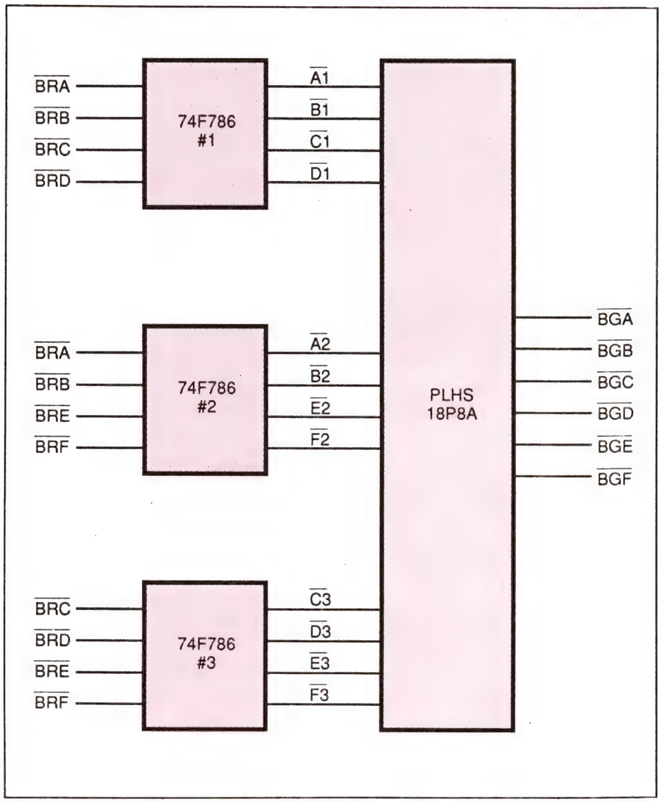


Fig 1b—By skillfully grouping the bus-request lines at a parallel array of bus-arbitration chips and using a PLD to perform a secondary arbitration, you can retain the 74F789's excellent metastability characteristics and still serve all inputs in order of arrival.

Routines give Quick Basic huge arrays

Steven B Leeland
Fairchild Data Corp, Scottsdale, AZ

The Quick Basic subroutine and function in **Listing 1** lets your programs read and write to a large array. Normally, Quick Basic's dynamic arrays can be no larger than 16k, 4-byte elements. The subroutine WriteLarge writes array elements; LargeArray reads them. You refer to elements as if they were normal subscripted variables. The main program is a simple test that verifies the unique existence of every array element.

To Vote For This Design, Circle No. 748

Listing 1—Quick Basic large-array routines

```
DECLARE SUB WriteLarge (address, value)
DECLARE FUNCTION LargeArray (address)

MaxLength = 16383                   'Maximal Length Dynamic Arrays
DIM LargeArray1(MaxLength)          (Outside DGroup)
DIM LargeArray2(MaxLength)
DIM LargeArray3(MaxLength)
DIM LargeArray4(MaxLength)

CLS

FOR address = 0 TO 65535                   'Large Array Convergence Test
        WriteLarge address, address        'Fill Array with Addresses
        LOCATE 8, 20
        PRINT "Filling array element: "; address;
NEXT

FOR address = 0 TO 65535                   'Test Results
        IF address = LargeArray(address) THEN
                LOCATE 16, 20
                PRINT "Testing array element: "; address;
        ELSE
                LOCATE 23, 20
                PRINT "Error at "; address; " = "; LargeArray(address);
        END IF
NEXT

END

FUNCTION LargeArray (address)
        SHARED LargeArray1(), LargeArray2(), LargeArray3(), LargeArray4()
        IF address < 16384 THEN
                LargeArray = LargeArray1(address)
        ELSEIF address < 32768 THEN
                LargeArray = LargeArray2(address - 16384)
        ELSEIF address < 49152 THEN
                LargeArray = LargeArray3(address - 32768)
        ELSE
                LargeArray = LargeArray4(address - 49152)
        END IF
END FUNCTION

SUB WriteLarge (address, value)
        SHARED LargeArray1(), LargeArray2(), LargeArray3(), LargeArray4()
        IF address < 16384 THEN
                LargeArray1(address) = value
        ELSEIF address < 32768 THEN
                LargeArray2(address - 16384) = value
        ELSEIF address < 49152 THEN
                LargeArray3(address - 32768) = value
        ELSE
                LargeArray4(address - 49152) = value
        END IF
END SUB
```

DESIGN NOTES

Number 30 in a series from Linear Technology Corporation January, 1990

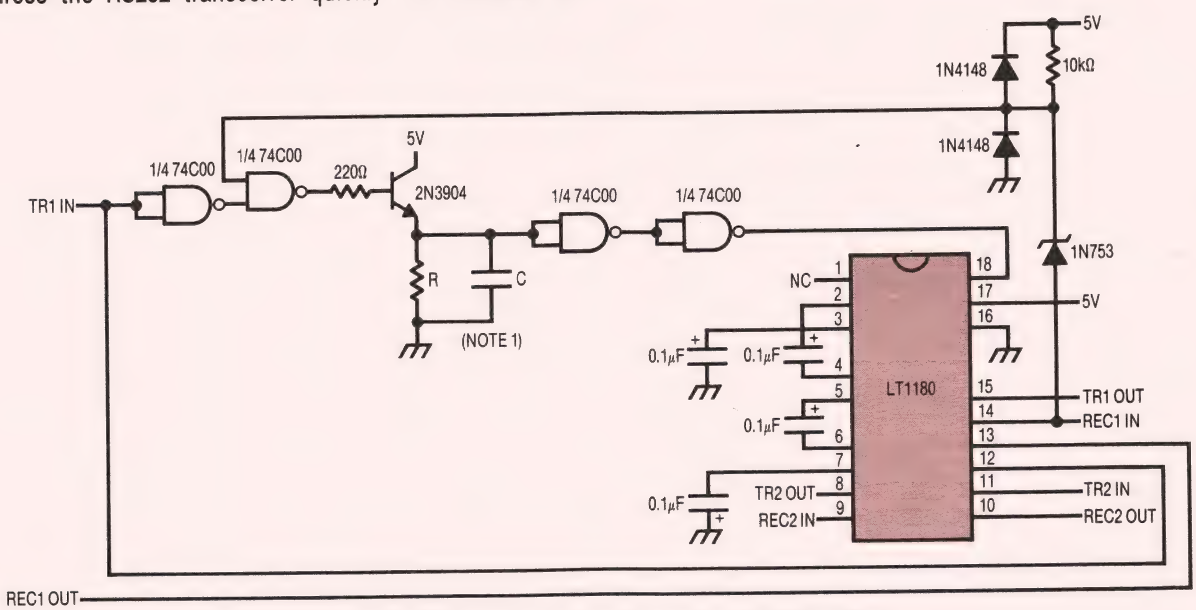
RS232 Transceiver with Automatic Power Shutdown Control

Sean Gold

The LT1180/81 RS232 transceivers with on-chip charge pumps offer some unique features that greatly enhance serial interface performance. Like the LT1080 and LT1130 series transceivers, the LT1180 is fully compliant with all RS232 specifications. The LT1180 is unique since it utilizes a charge pump which oscillates at 150kHz to 200kHz — about twice the frequency of the standard transceivers. In addition to providing excellent current delivery capability, the high speed charge pump can operate with storage capacitors as small as 0.1μF.

Reducing storage capacitor size to 0.1μF shrinks board space, thereby lowering production costs. Small capacitors also shorten the transceiver turn-on time to less than 200μs, which makes the LT1180 ideal for applications which must address the RS232 transceiver quickly. The interface described here takes advantage of fast turn-on to reduce power dissipation.

The circuit shown in Figure 1 automatically shuts down when there is no data flow through the interface. A data stream on either the RS232 or logic inputs activates the transceiver. The data must begin with a logic 1 preamble, and the data stream must contain a sufficient number of 1's to keep the transceiver active. The preamble may be as short as 50μs. Alternatively, the input to the Automatic SHUTDOWN circuit could be an RS232 handshake signal, such as Data Set Ready (DSR) or Clear to Send (CTS), which remain high during the data transfer. The LT1180's 200μs turn-on delay does not limit the data rate in the transceiver. Once the LT1180 is active, it can process data at the maximum 100k baud data rate.



NOTE 1: SELECT RC BASED ON CLOCK SPEED AND REQUIRED DROP OUT TIME. $\tau = RC \approx 2 \cdot T_{DROP\ OUT}$. FOR THIS EXAMPLE, R = 100KΩ AND C = 1μF. C SHOULD NOT EXCEED 1μF UNLESS THE 2N3904 CURRENT LIMITED WITH A COLLECTOR RESISTOR.

Figure 1. Fast Turn-On Transceiver with Automatic SHUTDOWN Control

A peak detector senses data flow. The extra CMOS gates are buffers which ensure the time constant is relatively independent of input signal level. The drop out time, i.e. the duration of inactivity prior to SHUTDOWN, is approximately 0.5RC. More specifically, drop out occurs when the voltage on the peak detector decays from $V_{CC} - 0.7V$ to the logic switch point of $V_{CC}/2$. The RS232 input to the control circuit is clamped to protect the logic inputs. The zener diode, D3, forces the turn-on threshold on the RS232 side to $-3.5V$, which prevents the transceiver from turning on when the cable is grounded.

Figures 2 through 4 demonstrate the automatic SHUTDOWN control's response to logic and RS232 signals, as well as zero data flow. The minimum pulse width is 50µs and the drop out time is set to 50ms. The power supply outputs — the lower two traces in Figures 2 and 3 — become active in less than 200µs. When active, the circuit consumes 16mA of quiescent current. In SHUTDOWN state, the Q-current drops to 50µA.

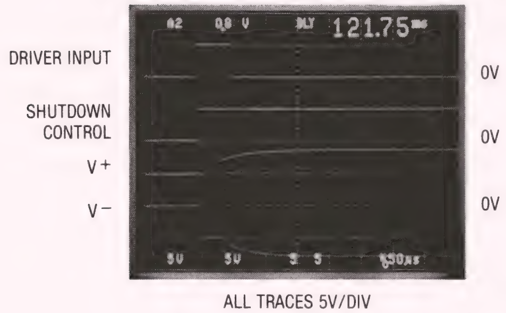


Figure 2. Transceiver Turn-On Via Logic Input

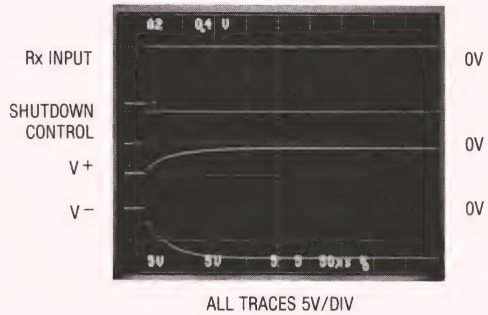


Figure 3. Transceiver Turn-On Via Receiver Input

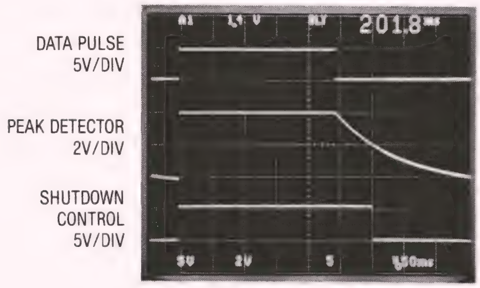


Figure 4. SHUTDOWN After 50ms Without Data Transmission

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IM/GP 1289 165K

Resistor isolates grounds

John Dunn
Bertan Associates, Hicksville, NY

System-design mavens insist that you should keep your analog and digital grounds completely separate except for one common point. However, if you're trying to lay out an IEEE-488 device, standard device-interconnection cables can foil your best intentions when their metal shells connect digital ground to your device's chassis; in effect, you'll have a ground loop as soon as you plug a cable into your device **(Fig 1)**.

In this case, your best bet is to use a resistor to connect the two grounds within your device. That way, any appreciable digital-ground currents will flow through the external path in the cable shell. It isn't a good idea to eliminate the 1Ω resistor and use the cable shell as the only ground path. Such a configuration causes a problem if you ever have to operate your device without the cable plugged in. EDN

To Vote For This Design, Circle No. 749

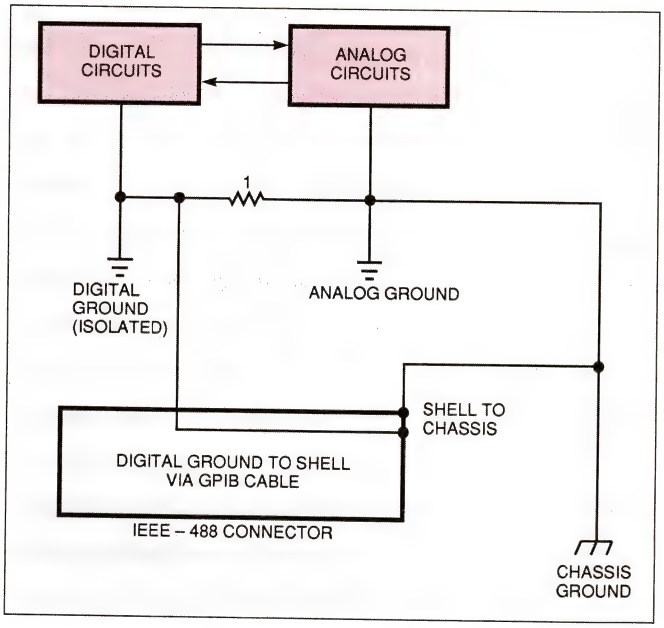

Fig 1—Connecting analog and digital grounds *with a 1Ω resistor kills a possible ground loop in IEEE-488 systems whose cables have metal connector shells that connect digital ground to your chassis.*

Op amp increases output impedance

Jimmy D Slife
XEL Communications Inc, Aurora, CO

Conventional op-amp circuits provide very low output impedances, but occasionally you may need a higher output impedance. One easy way to get your desired output impedance is simply putting that value resistor in series with the output of the op amp. Unfortunately, this scheme limits the op amp's output range.

For example, putting a 600Ω resistor in series with an op amp's output to achieve a 600Ω impedance would mean that for a 1V rms output, the op amp could deliver only about 420 μW to the load. The circuit in **Fig 1,** on the other hand, can use a much smaller output resistor and still have the 600Ω output impedance. For example, it would supply approximately 1.24 mW at the 1V output level using a 90Ω output resistor. This design is valid only for ~600Ω and ~90Ω.

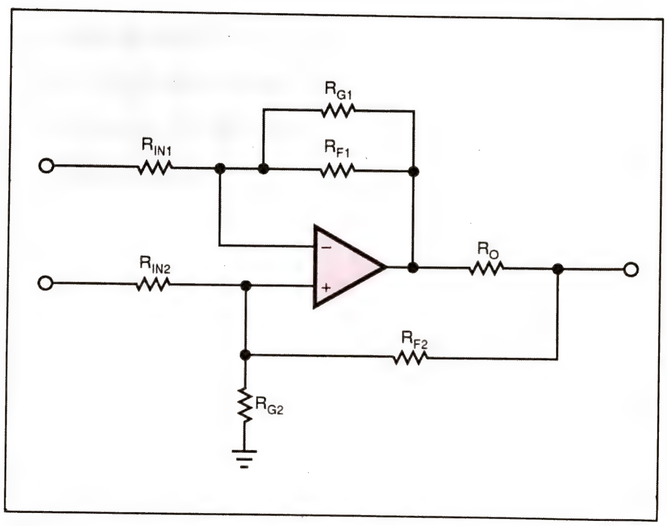

Fig 1—This op-amp circuit presents *a high-impedance output without dissipating excessive power in its series-output resistor.*

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ISSUE WINNER

The winning Design Idea for the October 26, 1989, issue is entitled "C program rotates vectors," submitted by Branko Zebec of PEL Electronics (Varazdin, Yugoslavia).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

The circuit's design equations are

$$\frac{V_O}{V_I}=\frac{R_G}{R_{IN}},$$

$$Z_O=R_O\left(\frac{R_G}{R_F}+1\right),$$

$$R_G=R_F\left(\frac{Z_O}{R_O}-1\right),$$

$$R_F=\frac{R_G}{\left(\frac{Z_O}{R_O}\right)-1}, \quad \text{and}$$

$$Z_O=\frac{V_O}{I_O}=\frac{R_GR_O(R_F+R_G)}{R_FR_G}.$$

The circuit can be inverting or noninverting. If you use the inverting configuration, combine R_{IN2} and R_{G2} into a single resistor. Also, you can usually combine R_{F1} and R_{G1} into a single resistor. EDN

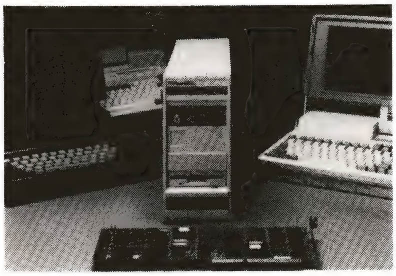
To Vote For This Design, Circle No. 750

Handheld Scanners For Macintosh Computers

- *400-dpi resolution on black-and-white documents*
- *3-color single-pass scanning for 4000 colors on color model*

The Model 400A and Model 270A are handheld scanners for Macintosh computers. The Model 400A provides 400-dpi resolution when scanning black-and-white documents. This model uses variable scanning methods, which create bayer, mesh, or spiral dithering patterns for monochrome line art. The unit has a scanning speed of 3.1 in./sec and a scan width of 4.1 in. A window on the scanner permits visual scan alignment. The Model 270A provides 3-color single-pass scanning for documents with as many as 4000 colors. The unit provides a resolution of 4 bits/color for each color. Its scanning speed is 1 in./sec, and it can scan color images that are 2.53 in. wide in a single pass. Both models have a switch to start scanning and variable intensity controls. They come with an external SCSI unit and connectors for interfacing with the Mac. Model 400A, $500; Model 270A, $800.

Accel Computer Corp, Von Karman Commerce Center, Suite 110, 17145 Von Karman Ave, Irvine, CA 92714. Phone (714) 757-1212. FAX 714-757-1288. **Circle No. 375**



Expansion Station For Laptop Computers

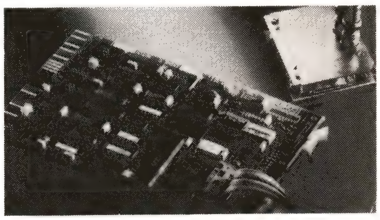
- *Three to five IBM PC, PC/XT, and PC/AT expansion slots*
- *Multiple bays house $3^1/_2$- and $5^1/_4$-in. storage devices*

The LapStation expansion unit provides laptop computers with the features of a desktop computer. The unit provides from three to five 8-or 16-bit IBM PC, PC/XT, or PC/AT expansion slots and multiple bays that can house 3½- and 5¼-in. storage devices such as hard-disk drives, streaming-tape drives, and floppy-disk drives. The unit comes with a Personality Adapter Kit that adapts the unit for operation with laptops from Sharp, Toshiba, Datavue, NEC, Epson, Hitachi, Compaq, Sanyo, Zenith, and Mitsubishi. The LapStation comes in two models and has a 3-ft interface cable that permits the unit to be placed behind a desk. $795.

Axionix Corp, 2257 S 1100 East, Suite 2C, Salt Lake City, UT 84106. Phone (800) 866-9797; in UT, (801) 866-9797. FAX 801-485-6204. **Circle No. 376**

Arcnet Adapter Board For DEC Computers

- *2k-byte RAM provides four 512k-byte packet buffers*
- *Acts as slave on 16-, 18-, and 22-bit versions of Q Bus*



The Q-ARC-01X Arcnet adapter board for MicroVAX, VAX II, PDP-11, and LSI-11 computers functions as an intelligent slave for 16-, 18-, and 22-bit versions of the Q Bus. The board uses a Standard Microsystems 9026 LAN controller IC and 2k bytes of RAM, which provide four 512-byte packet buffers. The packet buffers can send and receive in any combination. The buffer base address can be located on any 2048-byte boundary within the Q Bus address range, including the I/O space. The control and status-word base can be located on any 4M-byte boundary within the I/O page-address space. Drivers are available for the RSX-11M/M+ and VMS operating systems. A NetBIOS, endorsed by the Arcnet Trade Association, is also available

and permits the interconnection of VAX and ISA bus computers that use high-level software. The board also operates with Fast File Transfer software. $1995.

C&C Technology Inc, Bldg 9, Unit 60, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (312) 231-0015. **Circle No. 377**

Board For IBM PC, PC/XT, and PC/AT computers

- *Has 4-user interface using a single expansion slot*
- *Dedicated CPU and as much as 4M bytes of RAM/user*

The K-Slave/4 is a modular multiuser plug-in system for IBM PC, PC/XT, PC/AT, and compatible computers. A single-slot plug-in board accepts daughter modules to provide 4-user access to the computer's resources. The modules provide each user with a dedicated 8-MHz NEC V20 CPU and either 512k, 768k, or 1M byte of RAM. Of the 1M-byte memory, you can use 704k bytes for application software. In addition, the board provides features that push network overhead over the 704k-byte boundary. These features enable the implementation of memory-hungry software applications that typically require an extended or expanded memory board. You can also connect a display terminal through an RS-232C port. Base board with one daughter module, $400; additional daughter modules, $300 each.

Kimtron Corp, 1709 Junction Ct, Bldg 380, San Jose, CA 95112. Phone (408) 436-6550. FAX 408-436-1380. TLX 6975590.

Circle No. 378

X Window Terminal With MC68010 µP

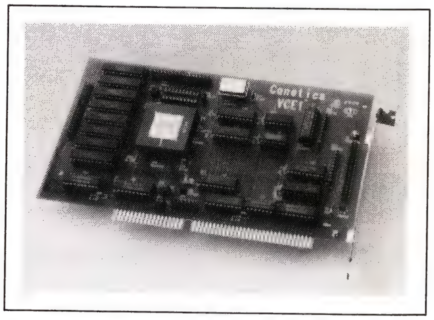
- *Applications for Unix, VMS, and Xenix*
- *Has an X server in EPROM based on the MIT X standard*

The QXT 10 X Windows terminal provides simultaneous access to networked computers that can be running X Windows applications using Unix, VMS, Xenix, and other operating systems. The terminal employs an MC68010 µP, and it has an X server in EPROM that's based on the MIT X, V11, release 3 stan-

dard. The QXT 10 comes with a flat-screen monitor and an enhanced PC/AT keyboard. The terminal's low-profile box, which contains the logic board and interconnects, fits directly under the monitor. Its logic board has an Ethernet interface, which supports TCP/IP (Transmission Control Protocol/Internet Protocol) and Telnet data-transfer network protocols. In addition, it provides VT 220 terminal emulation through an RS-232C interface. The terminal also has additional ports that interface with a local printer and an optional 3-button mouse. 1M-byte version with network interfaces, software, monitor, keyboard, and mouse, $1495.

Qume Corp, 500 Yosemite Dr, Milpitas, CA 95035. Phone (408) 942-4000. FAX 408-942-4052.

Circle No. 379



Vector-Processor Board For ISA Bus

- *Parallel addition and multiplication operations*
- *Delivers 12.5 MIPS and performs 32-bit floating-point math*

The VCE1 vector-processor board for the ISA bus uses an AT&T DSP32C DSP chip, which executes parallel multiplication and addition at 12.5 MIPS. The card performs 32-bit floating-point math, according to the IEEE format, as fast as 25M flops. Other features include 256k bytes of zero-wait-state RAM for program and data; daughter cards for as much as 16M bytes of memory expansion; DMA transfer rates between the host and the card at 2M to 4M bytes/sec; a 20M-byte data tranfer to an external interface; and an option for an analog I/O port. Benchmark results include a 1024-point complex FFT calculation in 3 msec and an FIR filter implementation with as many as 12M taps/sec. Fortran and C subroutine libraries are also available. 20M-flops version with 256k bytes of RAM, $1675; 25M-flops version with 256k bytes of RAM, $1995; C or Fortran libraries, $485; software development kit, $1500.

Canetics Inc, Box 70549, Pasadena, CA 91107. Phone (818) 584-0438. FAX 818-584-0439.

Circle No. 380

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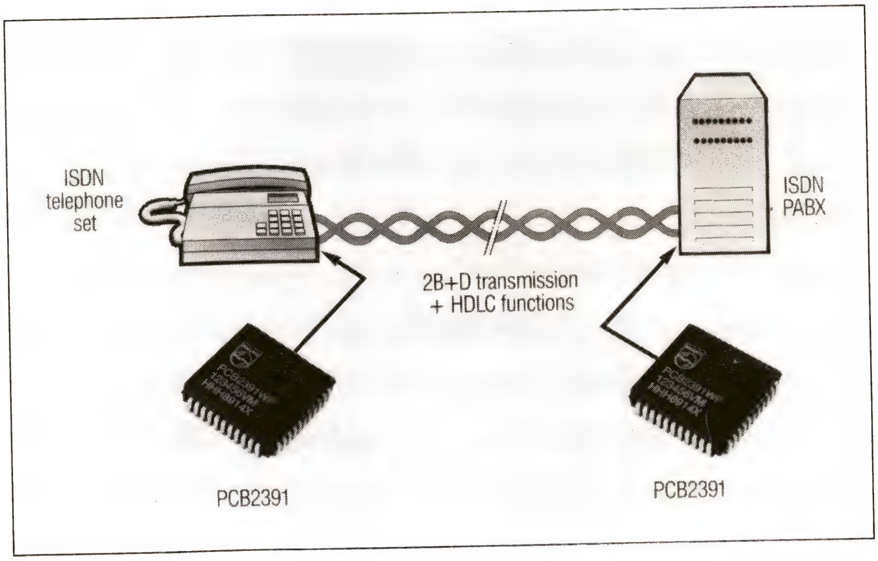

According to the company, the PCB2391 is the first single-chip ISDN (Integrated Services Digital Network) echo canceller to incorporate on-chip layer-2 functions. Optimized for PABX extension lines, the circuit also supports remote multiplexers and can operate in public exchange lines that serve nearby subscribers. The canceller is line-polarity independent and needs no active external components for sending on the line. Like most ISDN echo cancellers, the IC provides full-duplex transmission of 2B + D channels via normal twisted-pair wires. A 1B + D mode allows for time-slot saving on the exchange side. The PCB2391 provides a 2.048M-bps highway interface, which is compatible with standard codecs, using both long- and short-frame sync timing modes. On the line side, the IC uses a Manchester biphase code at a line rate of 152k bps. In a 44-pin PLCC (plastic leaded-chip carrier), $43 (1000).

Philips Components, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 724324. TLX 51573. **Circle No. 368**

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-4535. **Circle No. 369**

Switching Regulator

- *Has 3.5A output capability*
- *Operates over a 15-to-50V input range*

Featuring a high-efficiency DMOS power stage, the L4974 switching regulator has a 3.5A output capability. Housed in a 20-pin DIP that needs no heat sink, the device can deliver as much as 120W to the load. Heat is dissipated via a few square centimeters of printed-circuit copper. The regulated output voltage from the L4974 stepdown dc/dc converter is variable from 5.1 to 40V; the input range is 15 to 50V. Included in the switching regulator's circuitry are a 2% reference, current limiting, thermal protection, soft start, voltage feed-forward control, and reset and power-fail functions. $2.90 (5000).

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX 602-867-6290. **Circle No. 370**

Preregulator IC That Controls Power Factor

- *Offers power factors to 0.99*
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Offering a power factor as high as 0.99, the UC3854 family of preregulator ICs uses average-current control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak-current control, average-current control accurately maintains sinusoidal line current without slope compensation. The UC3854's high reference voltage and high oscillator amplitude minimize noise sensitivity, and fast pulse-width-modulation elements permit chopping frequencies above 200 kHz. The UC3854 operates from line voltages of 75 to 275V and from line frequencies of 50 to 400 Hz. Other features include fast feed-forward line regulation, a low-offset analog multiplier/divider, and a 0.5A totem-pole driver. In 16-pin plastic and ceramic DIPs, from $5.90 (100).

Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410. **Circle No. 371**

34-Channel Driver

- *Features push-pull output*
- *Has 250V rating*

Manufactured using the company's HVCMOS II process, the HV70 combines high-speed, low-power CMOS logic with 34 250V push-pull CMOS outputs on a single monolithic chip. The driver is a pin-compatible replacement for the Siliconix SI9560 and can also replace TI's SN75563 and SN75564 pair. The cascadable serial-to-parallel converter accepts 12V CMOS serial data and outputs it at 250V and 70 mA max at data rates in excess of 4 MHz. A direction pin allows data to flow either clockwise or counter-

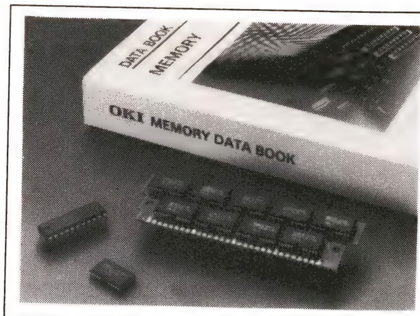
clockwise, which makes the HV70 particularly useful in display applications. Standby current is less than 50 nA. In plastic or ceramic J-lead packages, from $8.80 (1000).

Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94088. Phone (408) 744-0100. FAX 408-734-5247.

Circle No. 372

Space-Saving Memory Modules

- *Feature 4M-bit dynamic RAMs*
- *Have single in-line construction*



Using 4M-bit dynamic RAMs mounted on a small pc board, these single in-line memory modules (SIMMs) save space and reduce assembly costs. The SIMMs allow the user to plug large arrays of memories into the computer's main circuit board or a plug-in card. Existing 1M-bit modules can be replaced by the 4M-bit modules, reducing power consumption/bit by 75%, according to the company. The modules are organized as 4M×8 bits or 4M×9 bits. 4M×9-bit SIMM, $700 (1000); individual DRAMs in SOJ and DIP packages, from $75 (10,000).

Oki Semiconductor, 685 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 720-1900. **Circle No. 373**

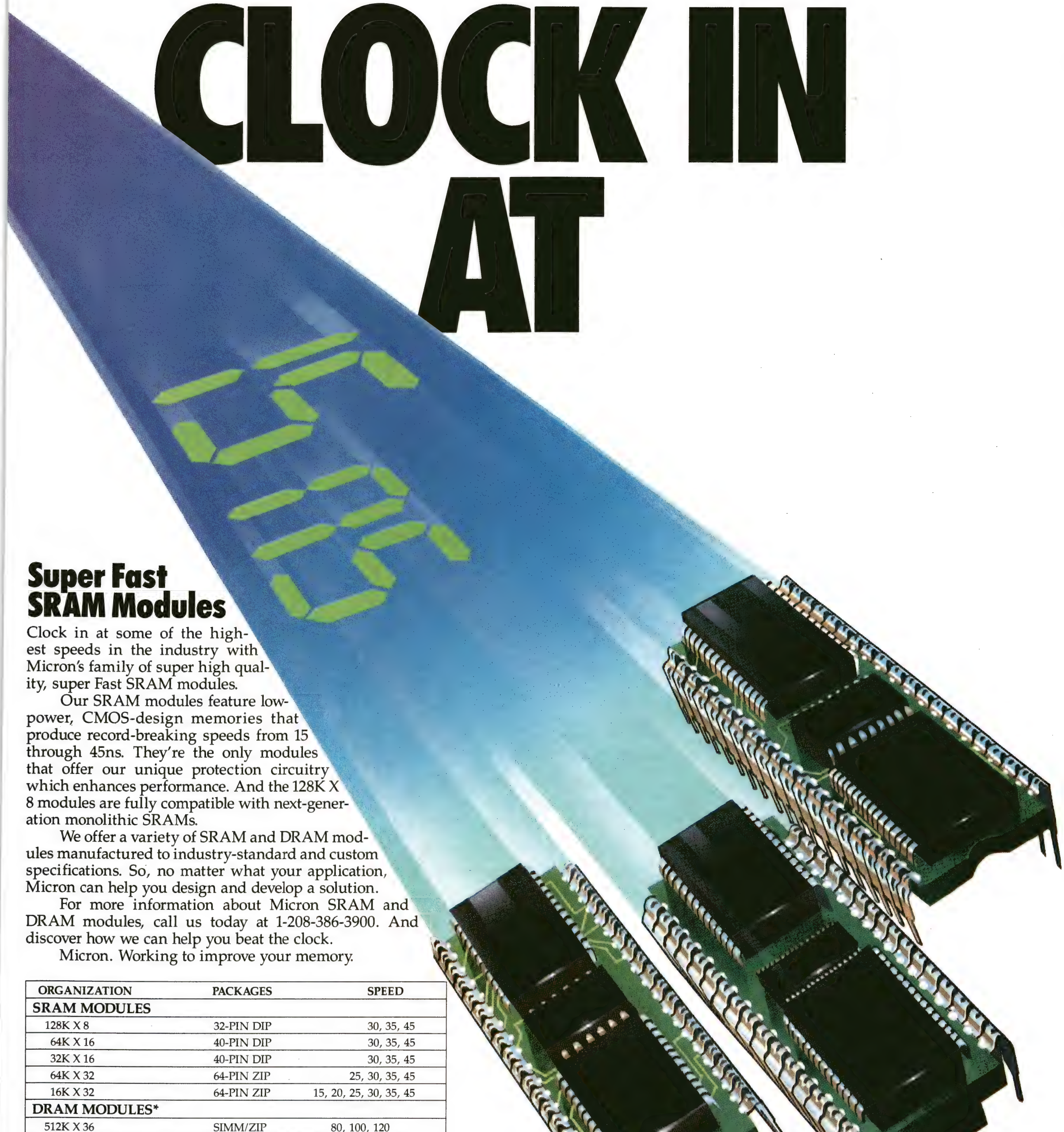
Dual BiFET Op Amp With Fast Settling Time

- *Settles to 0.01% in 500 nsec*
- *Has 13-MHz gain-bandwidth product*

A dual version of the popular AD744 precision op amp, the AD746 settles to 0.01% in 500 nsec for a 10V step, a speed that is three times faster than existing dual BiFET op amps, according to the company. Other dynamic specifications include a 13-MHz gain-bandwidth product, a 75V/µsec slew rate, and only 0.0001% total harmonic distortion. For dc performance, the op amp features a typical offset voltage of 0.3 mV (1.5 mV max) and input offset drift of 12 µV/°C. Open-loop gain is a minimum of 150V/mV and is typically 300V/mV. In 8-pin miniDIP, hermetically sealed ceramic-DIP, and surface-mount packages, from $4.25 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 658-9400. TWX 710-394-6577. **Circle No. 374**

CLOCK IN AT



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64K X 32	64-PIN ZIP	25, 30, 35, 45
16K X 32	64-PIN ZIP	15, 20, 25, 30, 35, 45
DRAM MODULES*		
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256K X 36	SIMM/ZIP	80, 100, 120
1MEG X 8/9	SIMM/SIP	80, 100, 120
256K X 8/9	SIMM/SIP	80, 100, 120, 150
64K X 8/9	SIMM/SIP	80, 100, 120, 150
64K X 4/5	SIMM/SIP	80, 100, 120, 150

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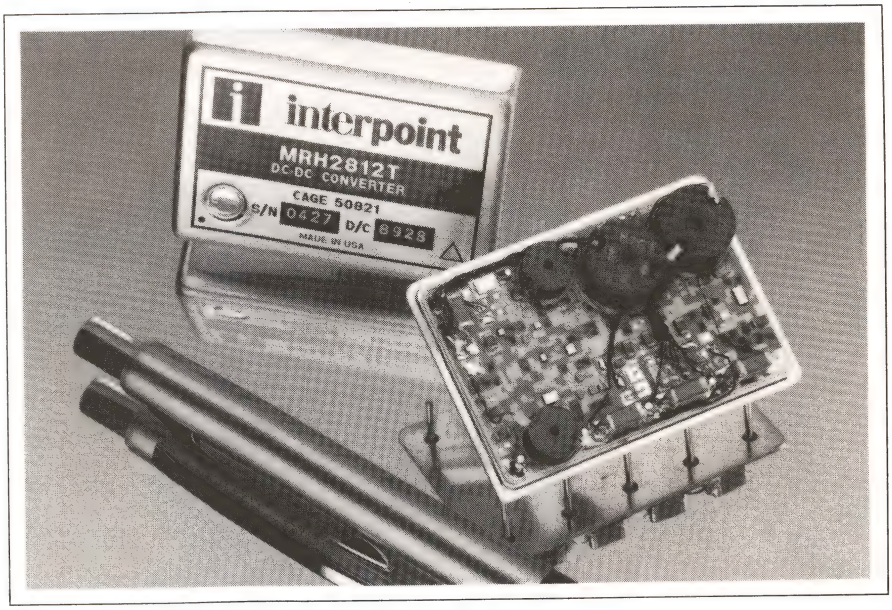
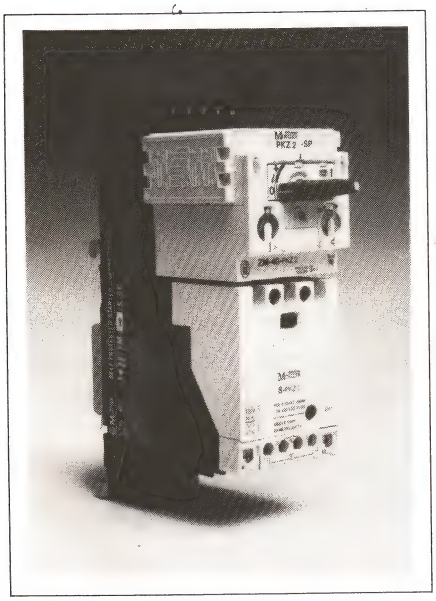
- *Radiation hardened*
- *Available with single, dual, or triple outputs*

MRH Series dc/dc converters will function through exposure to 10^{13} neutrons/cm^2, a 10^{11} rads/sec radiation dose rate, and a 10^5 rads total radiation dose. These 15W converters accept inputs of 16 to 36V and output 5, ±12, or ±15V in single-, dual-, and triple-output versions. Conversion efficiency equals 72%. Typical main output load regulation is 0.1%, and line regulation equals 0.05%. The multiple output models offer a flexible division of output power—the main output can handle from 2 to 10W, and each auxiliary will output from 0 to 6W. Worst-case start-up time measures 3 msec, and input-to-output ripple rejection equals −50 dB over the audio range. The units are housed in a hermetically sealed metal package that has a volume of just over 1 in^3. $667 (100).



Interpoint, Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX 206-882-1990.

Circle No. 354



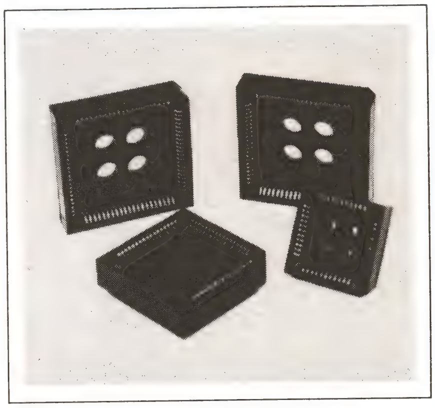
Self-Protecting Motor Controller

- *Has an interrupt rating of 65 kA at 480V ac*
- *Measures only 8×2.625 in.*

The PKZ 2-SP provides a number of functions—motor disconnect; motor branch-circuit protection; protection against short circuits, overloads, and ground faults; motor control; and self-protection under fault conditions. The basic unit, which measures 8×2.625 in., comprises disconnect, contactor, and trip modules. The controller has two sets of current-limiting main contacts: One single-break set provides disconnect and isolating functions; the other contact set provides the motor-switching capability. These contacts are functionally coordinated to minimize current and energy levels in the event of faults or short circuits. The plug-in trip modules, which come in 11 versions with ratings of 0.6 to 40A, take care of overloads and overcurrents and can handle motors rated for 30 hp at 460V. The PKZ 2-SP has an interrupt rating of 65 kA rms at 480V ac or 100 kA at 240V ac. From $446.

Klockner Moeller, 25 Forge Pkwy, Franklin, MA 02038. Phone (508) 520-7080. FAX 508-520-7084.

Circle No. 355



Chip-Carrier Sockets

- *Available in surface-mount versions*
- *Meet requirements of MIL-STD-202 and MIL-STD-1344*

These PLCC (plastic leaded chip carrier) sockets are available in standard- (−55 to +110°C) and high-temperature (−55 to +220°C) versions. In models with 20 to 100 positions, the sockets come in both through-hole and surface-mount types. Both types meet MIL-STD-202 and MIL-STD-1344 require-

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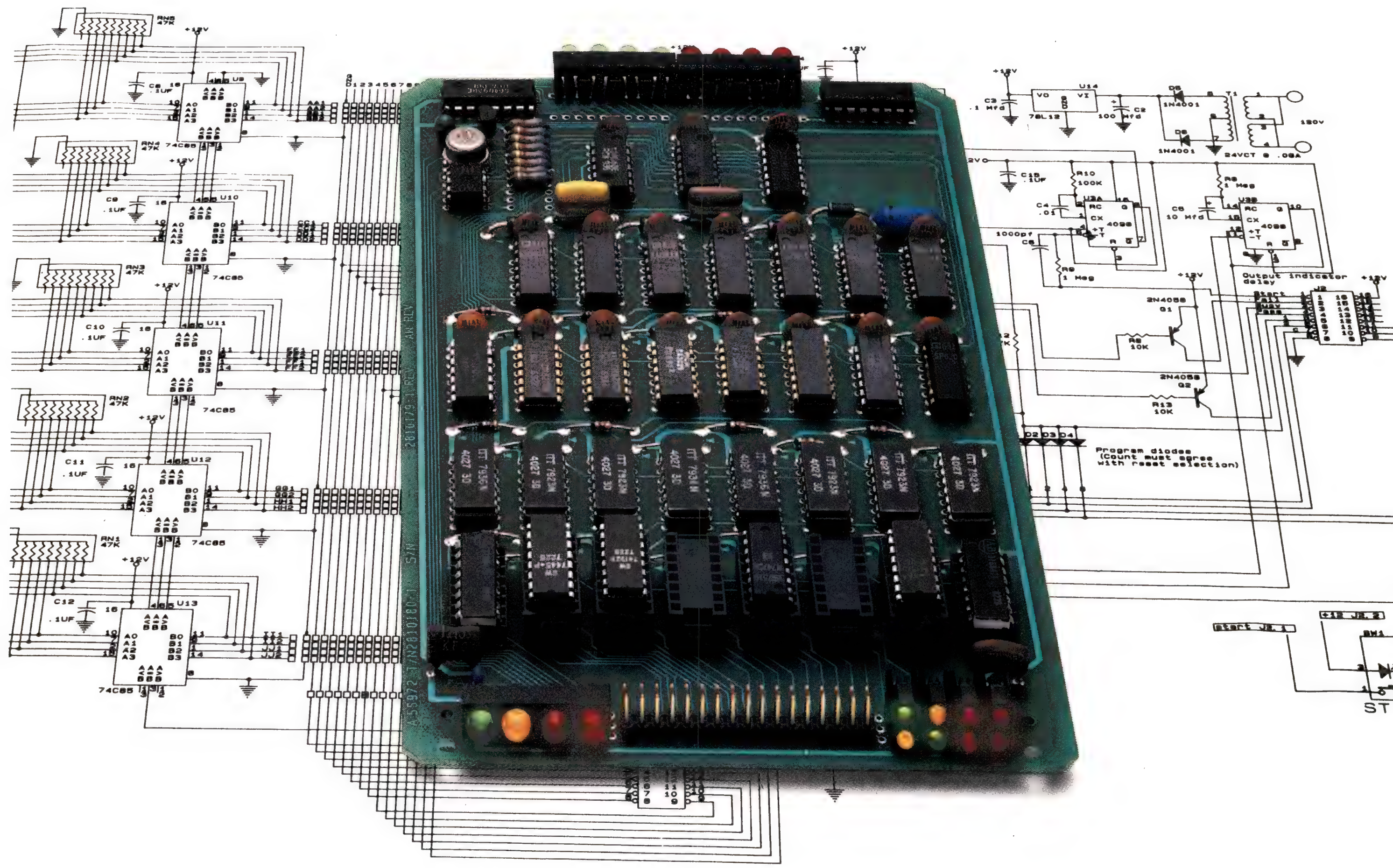

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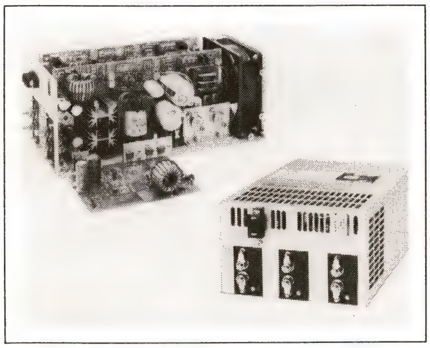
Industrial Devices, Inc. 260 Railroad Avenue, Hackensack, NJ 07601 (201) 489-8989 (201) 489-6911 (FAX)

CIRCLE NO. 118

ments. The sockets have terminations on a 0.1-in.-square grid. They are rated to carry 1A and have a withstanding voltage rating of 500V rms. From $1.50 (1000) for a 68-pin unit.

Arco Electronics Corp, 9016 Fullbright Ave, Chatsworth, CA 91311. Phone (818) 882-8707.

Circle No. 356



Triple-Output Power Supplies

- *Output to 1600W*
- *Have 82% efficiency*

Additions to the VF Series switching-power-supply family, these three models offer 5V at 120A on the main output and 12V ratings on auxiliaries to provide total output powers of 850, 1100, and 1600W. All three feature 82% typical efficiency, isolated regulated outputs, and VDE-, IEC-, UL-, and CSA-approved internal modules. An optional filter enables the supplies to meet FCC 20780 Part 15 Class A and VDE 0871/6 Class A for conducted emissions. $860 to $1260. Delivery, four to eight weeks ARO.

Deltron Inc, Box 1369, North Wales, PA 19454. Phone (215) 699-9261. TWX 510-661-8061.

Circle No. 357

Transmission Adapters

- *Let you mix serial and parallel devices*
- *Increase transmission distance to 4000 ft*

The Distance Extender family includes a series of parallel and serial adapters that extend the transmission distance between computers and peripherals using standard wire cable. Parallel models operate to 4000 ft at 56k bps/port over 2-pair wires; serial models provide the same distance gains at 115k bps over 4-pair wire cables. You can mix parallel and serial units in the same application. Models with Centronics 36-in. connectors and DB25 male plugs are available. From $110.

Digital Products Inc, 108 Water St, Watertown, MA 02172. Phone (800) 243-3333; in MA, (617) 924-1680. FAX 617-924-7814.

Circle No. 358

Pushbutton Switches

- *Available with silver- or gold-plated terminals*
- *Feature a 100,000-cycle life*

Measuring 0.156 in. deep by 0.36 in. in diameter, TL-360 pushbutton switches are well suited for pc-board-mount applications. They have a life of 100,000 cycles and feature oxygen-free copper terminals, which are available with silver or gold plating. Actuating force measures 25 oz max, and switch-travel figures range from 0.015 to 0.025 in. Maximum switch bounce equals 5 μsec. The switches are environmentally sealed against contamination during board-fluxing and -soldering operations. $0.49 (1000). Delivery, four to six weeks ARO.

Standard Grigsby Inc, 920 Rathbone Ave, Aurora, IL 60507. Phone (312) 844-4300. FAX 312-844-4286. **Circle No. 359**

Panel Indicators

- *Feature a large LED display*
- *Offer 1-count repeatability*

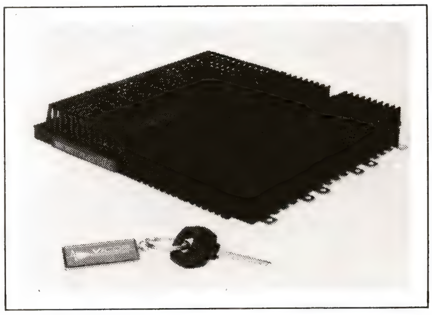
Units in the 400A Series of digital panel indicators have LED displays that feature 0.8-in.-high characters, which are readable from across a room. The indicators offer 3500- and 35,000-count resolution with 1-count repeatability. The units have temperature resolutions of 1, 0.1, and 0.01°; resolutions of 0.1 to 0.001 mV and 0.01 to 0.0001V are featured for dc measurements. A miniature DIP switch, accessible from the front panel, allows you to change between C and F measurements. Alarms, BCD output, and analog output are some of the plug-in options available. From $339.

Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. FAX 619-268-0172. **Circle No. 360**

Flat-Package Power Supplies

- *Offer tunable outputs*
- *Feature EMI/RFI filter*

The FlatPac family of user-definable off-line switching power supplies combines standard dc/dc converters with a set of modular-package and front-end subassemblies. Standard outputs are 5, 12, 15, 24, and 48V. All outputs are trimmable



by +10 and −100%. The supplies feature EMI/RFI filtering to VDE/FCC class A requirements and have safety-agency approvals pending. Sharing a common flat-package profile measuring 1.37×8.6 in., FlatPacs come in widths of 2.5, 4.9, and 7.4 in. and can supply as much as 200, 400, and 600W, respectively. From $0.85/W.

Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (508) 470-2900. FAX 508-475-6715. **Circle No. 361**

CAE & SOFTWARE DEVELOPMENT TOOLS

Ada For DOS 386

- *Runs on 80386-based computers under PC-DOS*
- *Shell displays Ada programs in tree form to show dependencies*

The TeleGen2 Ada program-development system runs on 80386-based computers under PC-DOS. The compiler generates native 32-bit 80386 code and comes with a source-level debugger; a global optimizer; a set of language tools that includes a cross-referencer, a source-dependency lister, and a source formatter; and TeleShell. TeleShell, a screen-oriented user interface, gives you window, menu, and text-icon access to all programming operations. It can display Ada programs in spreadsheet form or in a tree form that shows module dependencies and lets you move rapidly between multiple screen levels. The source-dependency lister produces a valid compilation-order list from programs that contain many source-code packages. $2995.

TeleSoft, 5959 Cornerstone Ct W, San Diego, CA 92121. Phone (619) 457-2700. **Circle No. 362**

C Compiler For RISC

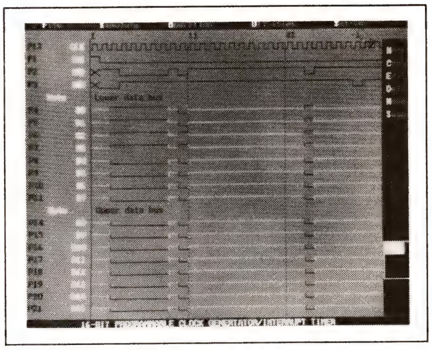
- *Works with Motorola 88000 RISC processor*
- *Conforms to ANSI X3J11 draft standard*

The D-CC/88K is a globally optimizing C cross-compiler for the Motorola 88100 RISC processor. The optimizations include automatic register allocations, reordering code scheduling, and global common-subexpression elimination. The compiler is compliant with 88-Open's Binary Compatibility Standard (BCS), and binary programs have successfully run on five different 88000-based computers. The compiler conforms to the proposed ANSI X3J11 C standard and accepts the standard Unix System V command-line options. It runs on a variety of host computers, including Sun workstations under Sun OS, DEC workstations under VAX/VMS or Ultrix, and Macintosh II under MPW. From $3500.

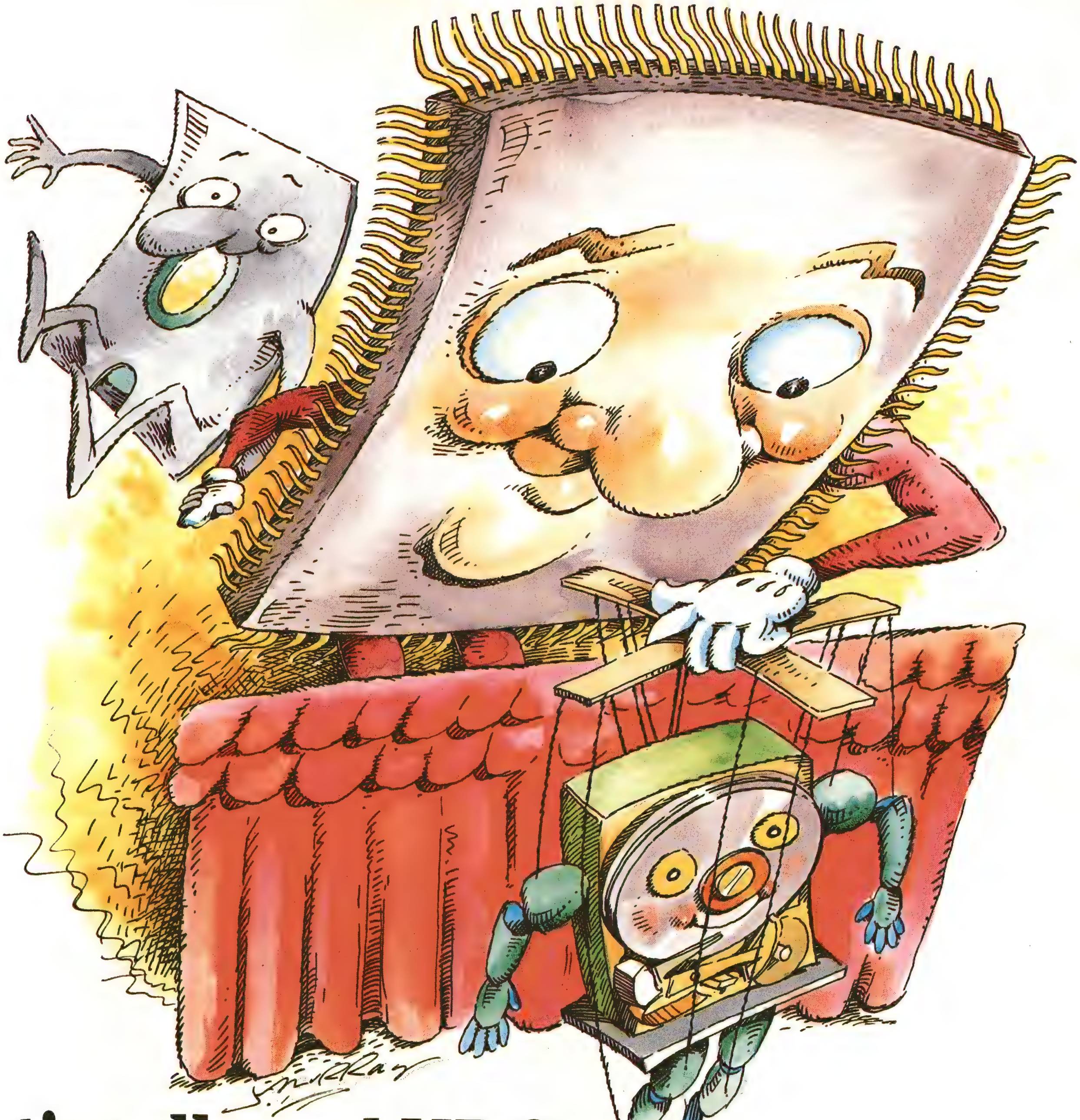
Diab Data Inc, 323 Vintage Park Dr, Foster City, CA 94404. Phone (415) 571-1700. **Circle No. 363**

Array-Design Tool

- *Helps you design high-density, multilevel circuits*
- *Allows Boolean-equation or state-machine data entry*



The PACE (PEEL Architectural Compiler/Editor) software package lets you design high-density, multilevel, I/O logic circuits for implementation in the vendor's line of PEEL (Programmable Electrically Erasable Logic) arrays. A mouse-driven graphics editor illustrates and controls the architecture of the particular chip you are using and makes the overall design easy to understand. It also allows you to define the logic by Boolean equations, state-machine terms, or a mixture of both. The built-in compiler transforms your logic and performs any one of five user-selectable levels of logic reduction. A simulator allows you to simulate both internal and external signals, and it generates a waveform-timing display for analysis. The package includes a direct interface to the vendor's PDS-1



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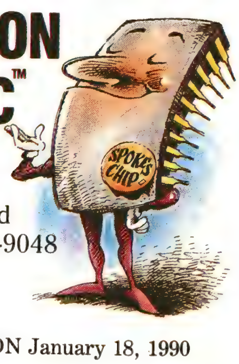


550 E. Brokaw Road
San Jose, CA 95161-9048
Tel: 408-441-1615
Fax: 408-954-0727

CIRCLE NO. 120

array programmer, as well as the ability to download data to Data I/O and other popular programmers. To run the design tool you need an IBM PC/XT, PC/AT, or compatible computer that has 640k bytes of memory, IBM EGA/VGA or compatible graphics, and a mouse. $695.

International CMOS Technology Inc, 2125 Lundy Ave, San Jose, CA 95131. Phone (408) 434-0678. **Circle No. 364**

Ada Development System For Transputers

- *Cross-compiler runs on DEC VAX computers*
- *Self-hosted compiler runs on Transputer board in IBM PC*

The company's Ada development system comes in two Transputer versions, both of which have been validated by the Ada Joint Program Office (AJPO). The cross-compiler runs on DEC VAX computers and generates code for the T8 Transputer; you can use the standard Occam tool set to download the executable code to the target processor. The self-hosted compiler runs on an auxiliary-processor board, which plugs into an IBM PC or compatible and is populated with T2, T4, or T8 transputers. You can run the executable code generated by the compiler on the auxiliary-processor board, using the I/O facilities of the PC; alternatively, you can download the code to a stand-alone Transputer system. Both compilers use standard optimization techniques, but in addition provide some Ada-specific optimizations, such as the elimination of redundant type-checking and the analysis of the call graph to eliminate uncalled code within a package. Self-hosted version, $22,250; DEC VAX cross-compiler version, from $30,000, depending on the host type and configuration.

Alsys Inc, 67 S Bedford St, Burlington, MA 01803. Phone (617) 270-0030. **Circle No. 365**

Telecomm Simulator

- *Simulates mixed analog and digital systems at block level*
- *Library has models of blocks for communications equipment*

TESS (Transient Electronic System Simulator) simulates mixed analog and digital systems at the block level. In particular, you can simulate microwave-radio and TV-transmission systems, codecs, PLLs, and most types of modulation. You can generate the free-format, Spice-like netlist with your text editor, which you can run from within TESS. For complex systems, you can use subcircuit models from the library of devices, including filters, mixers, and VCOs. You can also capture schematics created by CAE tools from OrCAD or P-CAD. To facilitate your use of these tools, the vendor can supply optional parts libraries of communication devices. The program can handle as many as 800 blocks and 1000 nodes and can make use of a numeric coprocessor, if your computer has one. TESS performs simulation on all blocks concurrently, with no restrictions on feedback loops. For spectrum analysis, you have control over the resolution, span, and averaging; you can use FFTs with as many as 4096 points. In order to tweak the design without editing the circuit file, you can substitute your own parameter names for the model parameter values. TESS simulator, $495; ModGen model generator, $245; parts library for OrCAD SDT III, $145; parts library for P-CAD MD-3, $225. Educational institutions can obtain site licenses for 20 users at the price of two copies.

Tesoft, 205 Crossing Creek Ct, Roswell, GA 30076. Phone (404) 751-9785. FAX 404-664-5817. **Circle No. 366**

ASIC-Design Synthesizer

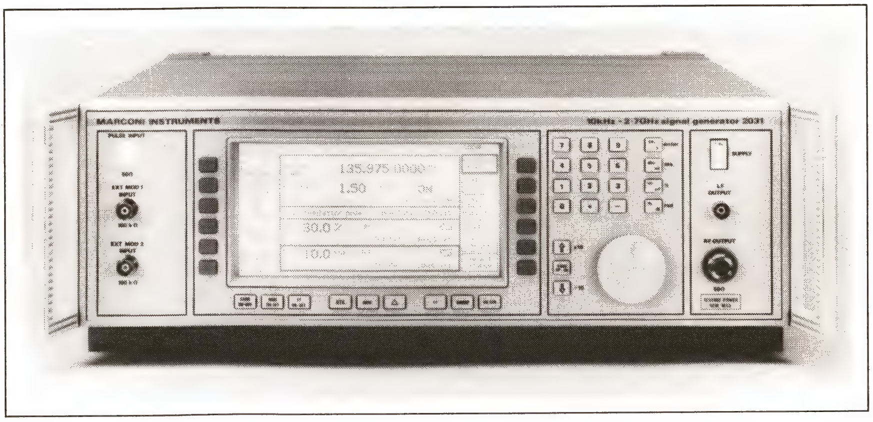
- *Accepts input in VHDL or the Verilog language*
- *Produces a complete ASIC design you can fabricate in silicon*

The ASIC Synthesizer will synthesize a complete ASIC design that you can fabricate in silicon. The package can accept input in either VHDL (VHSIC Hardware Description Language) or in Gateway's Verilog hardware-description language. Your design can be in the form of gate arrays, standard cells, or optimized cell-based designs. The tool can evaluate the HDL description and determine the best solution for a particular set of constraints. By using product-specific compilers, the ASIC Synthesizer can implement a datapath, multiplier, and memory; by using the logic synthesizer, it can implement general-purpose logic. The tool will be released in three phases: Phase 1 (currently available) lets you synthesize complete chips, including I/O pad ring, logic, datapaths, and memories, using a combination of behavioral and structural descriptions within the HDL; phase 2 (to be released in 1990) will recognize datapaths from the behavior within an HDL; and phase 3 (to be released in 1990) will recognize memory and other sequential elements, as well as datapaths. $100,000.

VLSI Technology Inc, 1109 McKay Dr, San Jose, CA 95131. Phone (408) 434-3000. FAX 408-263-2511. **Circle No. 367**

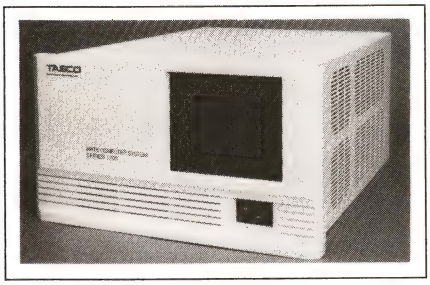
10-kHz to 1.35- and 2.7-GHz Signal Generators

- *Provide LCDs with fluorescent backlighting*
- *Step between frequencies in 1 msec*



The 2030 signal generator covers frequencies from 10 kHz to 1.35 GHz; the 2031 extends the range to 2.7 GHz. Both units provide 0.1-Hz resolution. They incorporate a digitally controlled sweep capability and can step to a new frequency in 1 msec. You can adjust the RF output level of either instrument from −144 to +13 dBm with an accuracy of ±1 dB. Optionally, the 2030's output extends to +19 dBm. The generators' user interface is based on menus that appear on a super-twist-LCD panel with fluorescent backlighting. The instruments allow modulation of their outputs with four simultaneous signals. Among the modulation modes are wideband FM, which on the 2031 allows 27-MHz deviation, and optional pulse modulation with 15-nsec rise and fall times. From $11,500. Delivery, six weeks ARO.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Phone (201) 934-9050. FAX 201-934-9229. **Circle No. 381**

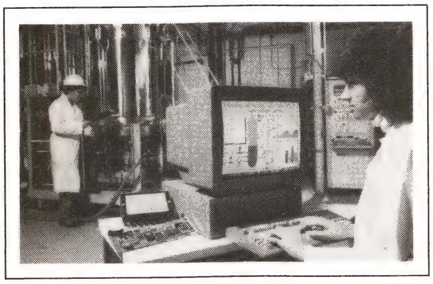


MATE-Compliant Computer System

- *Includes hardware and software*
- *Expands by adding VME boards and 5¼-in. peripherals*

The MCS-1700 computer system complies with the Air Force's MATE (Modular Automatic Test Equipment) standard. The hardware/software package is based on the MIL-STD-1750A instruction-set architecture. The CPU uses VME-bus boards and, therefore, expands in a modular fashion. The storage bays accommodate half-height 5¼-in. peripherals, making possible further modular expansion. The operating system, which is based on the MATE 5.0 operating system, supports four IEEE-488 buses and two SCSI disk drives. $39,500.

Tasco Electronic Services Inc, 2121 W Crescent Ave, Anaheim, CA 92801. Phone (714) 635-0550. FAX 714-535-3458. **Circle No. 382**



Two Analog-I/O Cards

- *One accepts 64 analog inputs*
- *Both provide 16 analog outputs*

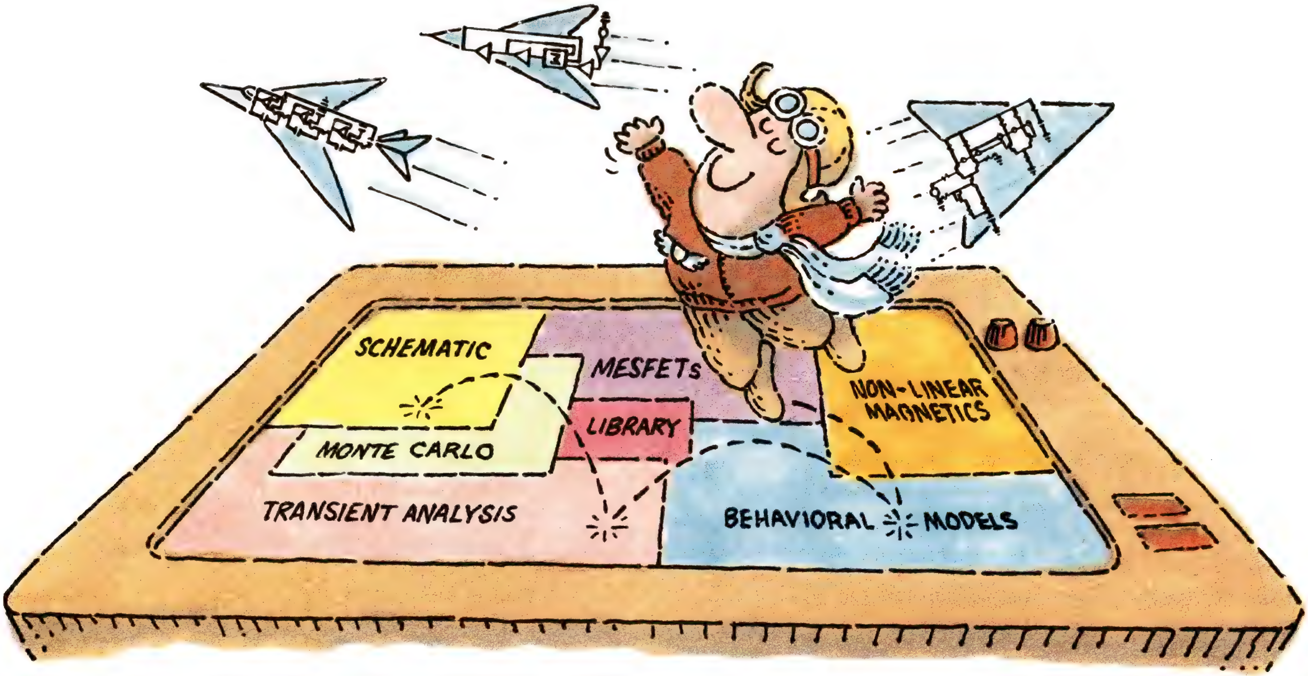
The RTI-220 analog-I/O board and the RTI-222 analog-output board plug into the IBM Micro Channel Architecture (MCA) bus. Each board provides 16 12-bit-resolution analog outputs derived from a single D/A converter; the RTI 220 also accepts 64 analog inputs and includes a 12-bit ADC capable of 21k conversions/sec. By use of external signal-conditioning panels, the boards can provide either voltage or current outputs and can provide 1500V isolation between the computer-system ground and the loads. The vendor provides software drivers for several interpreted and compiled high-level languages, including Basic, Pascal, and C. RTI 220, $650; RTI 222, $450 (1 to 9).

Analog Devices Inc, 70 Shawmut Rd, Canton, MA 02121. Phone (800) 426-2564. **Circle No. 383**

50V Pulse Generator

- *Provides 500-psec rise and fall times*
- *Produces pulses 20 nsec to 5 μsec wide*

The AVR-E2-C pulse generator produces 50V pulses with a rise and fall time of 500 psec and a width that you vary in two ranges from 20 nsec to 5 μsec. The maximum pulse rate is 50 kHz. Companion models produce 20V pulses with 300-psec rise and fall times to 100 kHz and 100V pulses with 500-psec transitions to 20 kHz. The genera-



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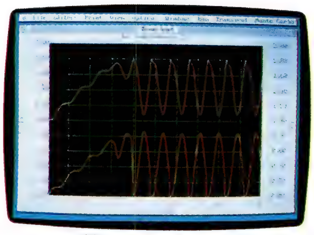
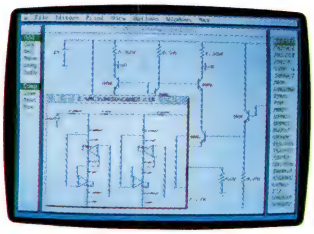
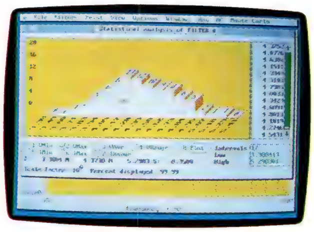


Transient analysis



Schematic editor



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And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

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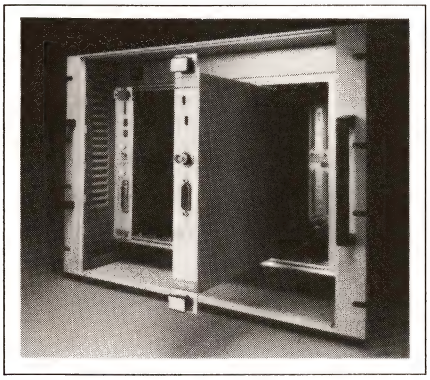
(408) 738-4387

CIRCLE NO. 121

tors are available as ac-powered, stand-alone, benchtop units and as 1.7×2.6×4.2-in. modules that use 24V dc power and require an external TTL trigger. An optional terminal allows the insertion of dc offset voltages to ±25V. $3552. Delivery, 60 days ARO.

Avtech Electrosystems Ltd, Box 265, Ogdensburg, NY 13669. Phone (315) 472-5270. **Circle No. 384**



6½-Digit VXIbus DMM

- *Fits in single-slot C-size module*
- *Incorporates isolated input to maximize noise rejection*

The 1362 is a 6½-digit multimeter in a single-width, C-size VXIbus module. The unit enables systems based on the open-architecture instrumentation bus to make precise, accurate measurements of resistance and ac and dc voltage and current. To minimize the effects of noise originating in the digital portion of VXI systems, the meter has an isolated front end that makes possible a common-mode rejection ratio of 146 dB at dc, and when the integration period is synchronized with the ac line, the ratio is 134 dB at 50, 60, or 400 Hz. Normal-mode filtering can reduce line-frequency-related errors by an additional 20 dB. As a 6-digit dc instrument, the meter makes 5 readings/sec; with resolution reduced to four digits, the unit makes 1000 readings/sec. The dc-voltage accuracy is 5 ppm of reading plus 2 ppm of full scale on the 10V range at 23 ±1°C for 24 hours after calibration. Under the same conditions, the ac-voltage accuracy is 0.02% of reading plus 0.01% of full scale from 40 Hz to 20 kHz. $3695. Model 1362MT, compatible with the MATE (Modular Automatic Test Equipment) standard, $3995. Delivery, six to eight weeks ARO.

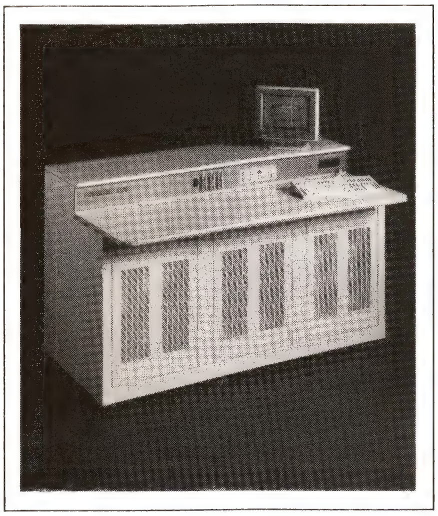
Datron Instruments Ltd, Hurricane Way, Norwich Airport, Norwich NR6 6JB, UK. Phone (0603) 404824. **Circle No. 385**

Wavetek Corp, 9045 Balboa Ave, San Diego, CA 92123. Phone (619) 565-9234. FAX 619-565-9558. **Circle No. 386**

VXIbus-Based Power-Supply Tester

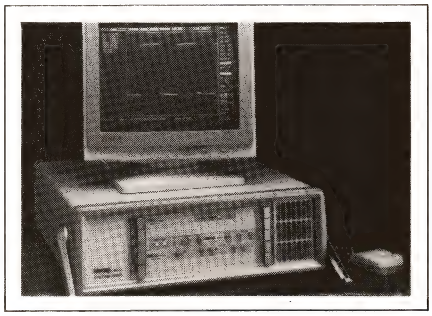
- *Includes ac and dc sources and electronic loads*
- *Has a multiplexer with 100-MHz bandwidth*

The Powertest 8100I is a power-supply tester based on the VXIbus,



an open-architecture instrumentation bus derived from the VMEbus. The system can include single- and 3-phase ac sources, dc sources, and 500 and 2500W, high-current electronic loads. The loads, which you can connect in parallel for increased dissipation, operate in constant-current and -resistance modes and contain voltage- and current-metering circuits. Because of its open architecture, you can configure the system according to your requirements and keep it up to date as those requirements change. A frequency-selective voltmeter module measures peak and peak-to-peak voltages in seven frequency bands, and a peak detector/timer measures transient response with 100-nsec precision. From $50,000. Delivery, 90 to 120 days ARO.

NH Research Inc, 16601 Hale Ave, Irvine, CA 92714. Phone (714) 474-3900. FAX 714-474-7062. **Circle No. 387**



2G-Sample/Sec Waveform Digitizer

- *Provides 63.5-dB (10.5-bit) dynamic range*
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The Series 2000 VMEbus-based waveform digitizer contains four 500M-sample/sec ADCs, each with a 330-MHz analog bandwidth; a 2k-word acquisition memory; and the ability to digitize with a signal-to-noise ratio of 63.5 dB (the equivalent of 10.5 bits). You can also configure the converters to acquire two signals at 1G sample/sec with 4k words of memory or one signal at 2G samples/sec with an 8k-word memory. You can expand the unit to contain 12 sampling modules with a total of 48 ADCs. A system with four channels and a 14-in. monitor costs $22,500. Additional 4-channel modules, $9950 each. Delivery, eight weeks ARO.

Analytek Ltd, 10261 Bubb Rd, Cupertino, CA. Phone (800) 366-5060; in CA, (408) 725-2560. **Circle No. 388**

Heat sinks and extrusions surveyed

This 112-pg catalog describes the vendor's complete line of stamped and extruded heat sinks and accessories. The publication discusses a variety of shapes that handle various space requirements and heat-dissipation needs. The book contains a new parts-numbering system and highlights technical data on heat-sink selection, analyzing thermal performance, and labor-saving options. Among the thermal-management products described are capacitor clamps and brackets, "hockey-puck" clamps, spring clips, forced convection coolers, Quik Connect dual terminals, mounting insulators, washers and grounding lugs, and thermal-conductive adhesives and compounds.

Aavid Engineering Inc, Box 400, Laconia, NH 03247.
Circle No. 351

Two books detail two versions of Turbo Pascal

Turbo Pascal DiskTutor and *Object-Oriented Turbo Pascal: A new paradigm for problem solving and programming* provide comprehensive tutorials to help you learn object-oriented programming with the vendor's Turbo Pascal. *Turbo Pascal DiskTutor* includes an updated version of Turbo Pascal 5.5, programming examples on disk, and a written tutorial providing complete instructions for learning Turbo-Pascal programming on your own. This version sells for $39.95. The second book, *Object-Oriented Turbo Pascal*, is aimed at classroom instruction and costs $9.95. A supplemental instructor's manual and a tutorial disk containing programming examples are available separately.

Borland International Inc, Box 660001, Scotts Valley, CA 95066.
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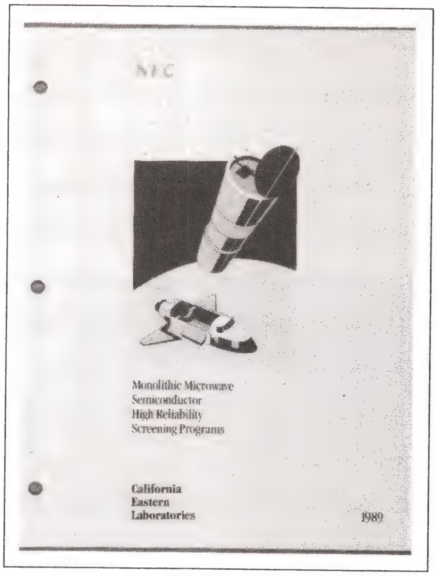

Screening procedure eases selection of ICs

The company's brochure describes screening and qualification procedures for NEC silicon monolithic-microwave ICs (MMICs), GaAs MMICs, and high-speed digital GaAs ICs. Also included are circuit elements such as transistors and resistors that meet MIL-STD-883. Reliability data for both chips and packages is presented for four grades: NEC Grade B—high reliability; NEC Grade C—military; NEC Grade CX—military; and NEC Grade D—industrial. Through the use of detailed processing information and flow diagrams, the brochure makes it easy to select reliability grades and complete specification-control drawings.

California Eastern Laboratories Inc, 3260 Jay St, Santa Clara, CA 95054.
Circle No. 352

Publication describes digitizing oscilloscopes

This brochure presents the Model HP 54120 Series digitizing oscilloscopes and time-domain reflectometry (TDR). The 34-pg publication discusses state-of-the-art applications and measurements, the Series' performance for computer-aided test applications, TDR, and the inside workings of the scopes, as well numerous accessories. The 4-color booklet features the latest model, the 34-GHz HP 54123T.

Hewlett-Packard, Box 2197, Colorado Springs, CO 80901.
Circle No. 353

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Doctor Design's SuperSpec, a subscription service, contains tables of composite specifications from 12 manufacturers for 80-, 100-, 120-, and 150-nsec, 1M-bit dynamic RAMs (DRAMs) operating in a 1-pg mode. The publication provides a composite specification that lists every timing parameter for each manufacturer and a worst-case composite value. The product also gives basic information about the working of DRAMs, their timing cycles, and their design parameters, and shows how to derive the DRAMs' composite specifications. The vendor supplies a 3-ring binder to hold the periodic updates. $195.

Academic Press, Harcourt Brace Jovanovich, Publishers, 1250 Sixth Ave, San Diego, CA 92101.
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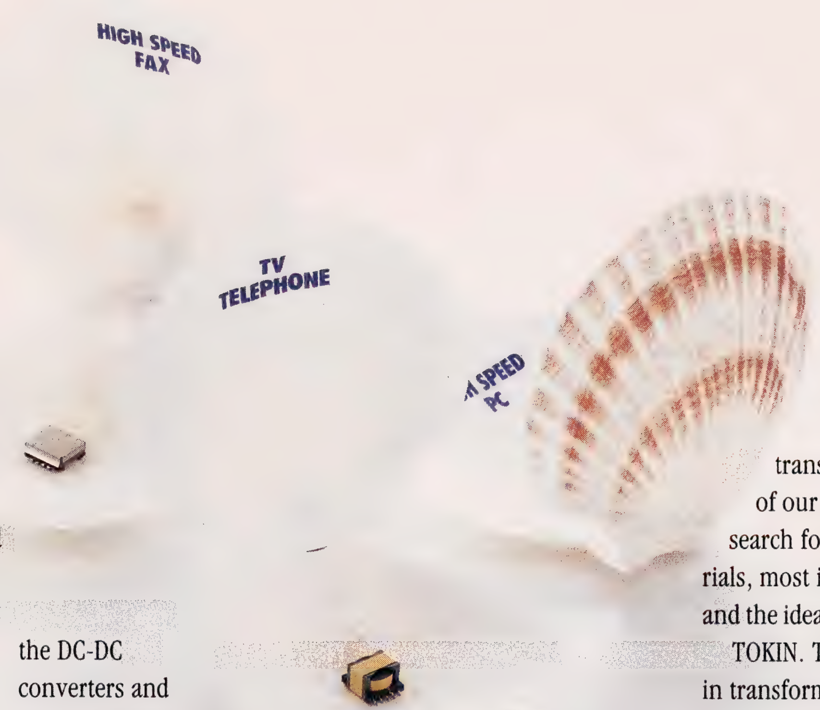

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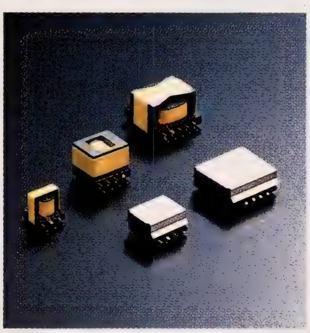

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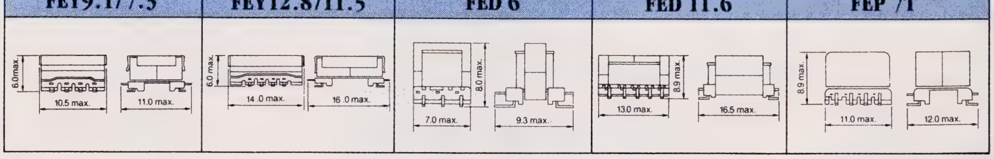

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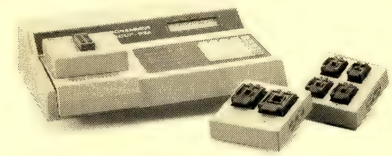

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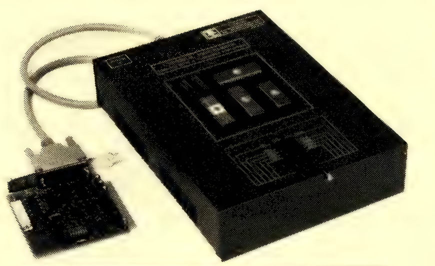

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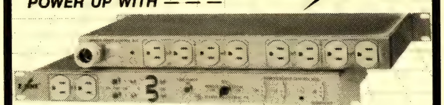

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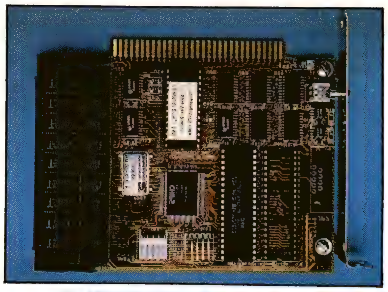

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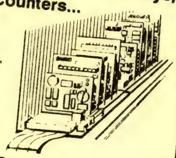

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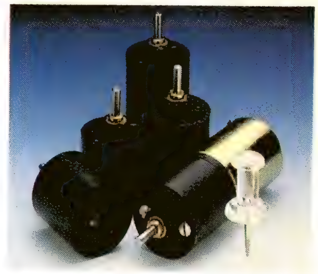

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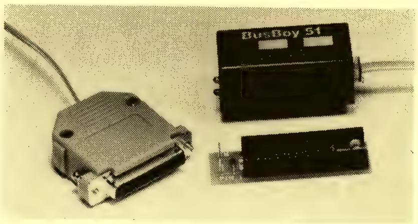

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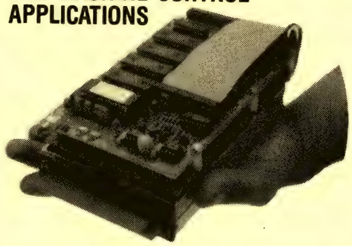

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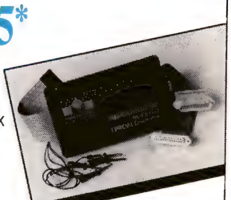

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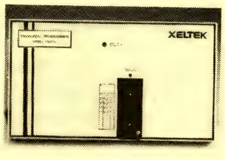

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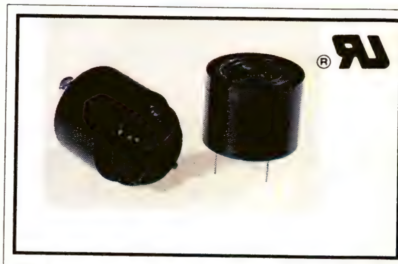

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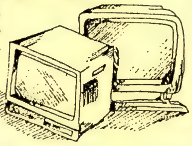

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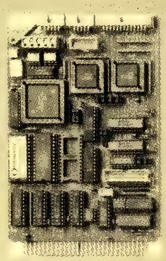

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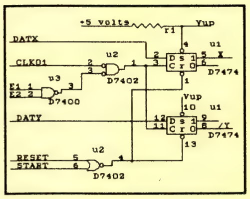

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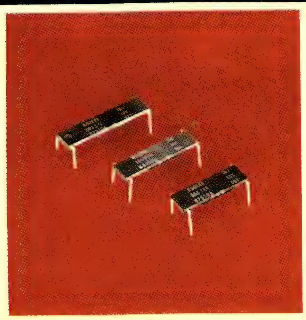

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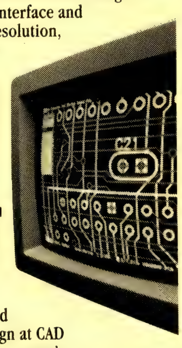

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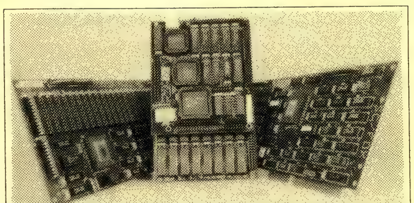

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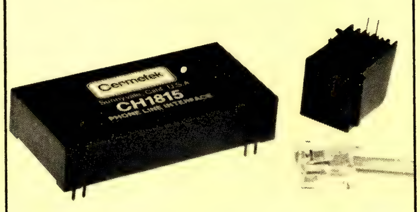

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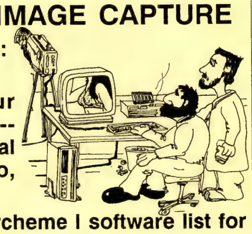

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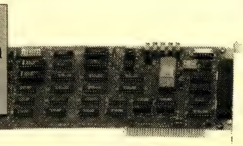

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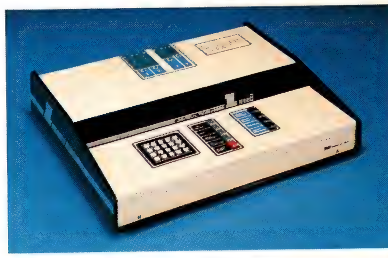

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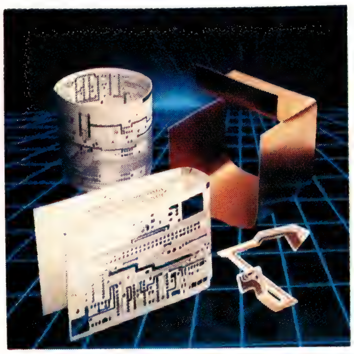

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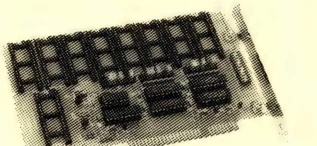

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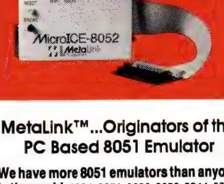

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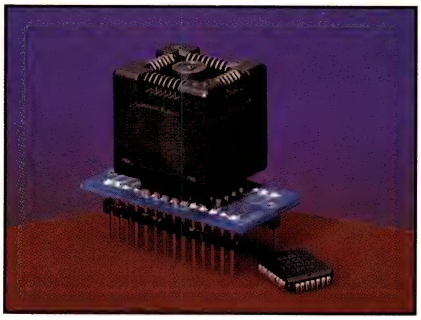

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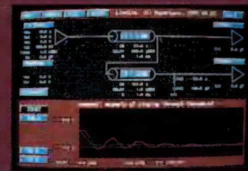

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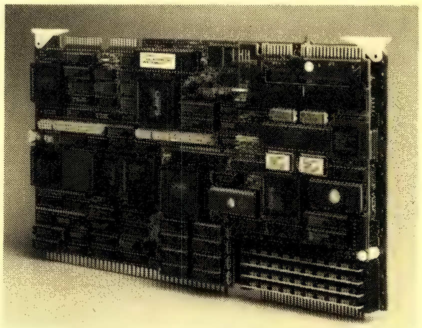

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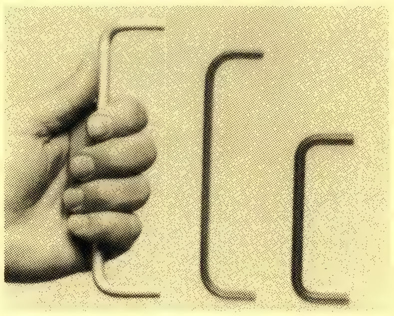

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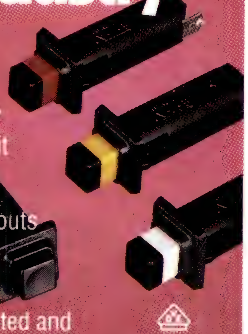

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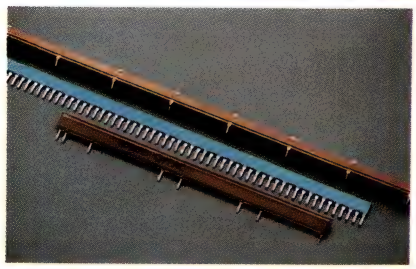

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The new headhunters

Jay Fraser, Associate Editor

They've been called personnel consultants, executive recruiters, and headhunters. They've also been called a variety of unprintable names. Depending on your point of view, they're either the people who help professionals advance their careers through judicious job changes or the people who raid companies and steal some of their best talent. Almost no one feels neutral about them.

Headhunters work differently than ordinary employment counselors. Employment counselors start with people who are looking for work and try to find jobs for them. Headhunters start with positions that are open and try to find qualified people to fill them.

They're knowledgeable.
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The client companies pay the headhunters' fees. The standard fee is 10% of the candidate's first-year salary, but that can go higher, especially if the position is for a high-ranking corporate executive whose salary is in six figures.

Headhunters acquired an unsavory reputation in the high-tech industry during the late '60s and early '70s. In those boom times new companies were being started every day and established firms were expanding rapidly. Qualified engineers were in short supply, and companies were willing to pay high prices to anyone who could bring them in. That situation attracted some people to the recruiting profession who were much more interested in fast money than in career guidance.

Some shady operators were known to run want ads for jobs that

Jim Lambrenos

didn't exist so they could build up a stock of resumes. Others would get a company telephone book and cold call all the engineers in it, trying to lure them away. Some headhunters didn't interview candidates or check references. They just sent dozens of semiqualified people to companies, hoping a few would be hired.

"Probably the thing that upset client companies the most was recruiting firms that were placing a candidate with a company, collecting the fee, then three or four months later taking that person out and moving him to another company," says Bob Read, who owns and operates a franchise of Management Recruiters in Redwood City, CA. "You've only got to do that a couple of times to lose all credibility with a client."

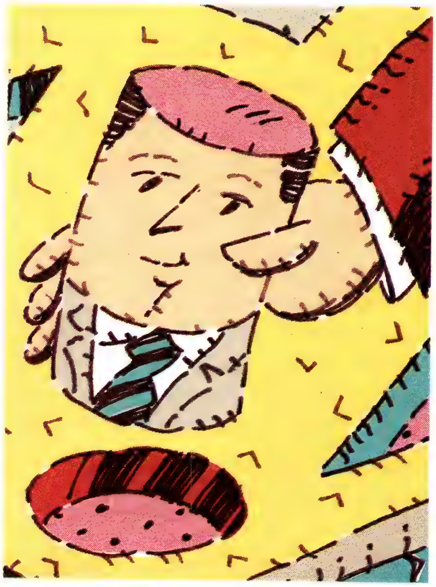
In 1969, Read, who has a degree in civil engineering from Iowa State University, went to a recruitment firm in San Francisco hoping it could find a position for him. He ended up going to work for it. "It's now 20 years later, and I'm still looking for the right position," he says with a smile. At one time he was the manager of eight recruitment offices in the Bay Area, and he has seen the profession change dramatically over the last two decades.

Early years of headhunting

"For the first three or four years that I was in the industry people would ask me what I was doing, and I'd say, 'Well . . . er . . . um . . . I'm a consultant or I'm this or I'm that'—anything but a headhunter," says Read.

However, with the shake out in the high-tech industry in the late '70s came a shake out in the ranks of the recruiters. Today's headhunters are much more professional and knowledgeable, and the word "headhunter" has lost most of its unpleasant connotations.

"We've cleaned up our image an awful lot in the last ten years," Read adds. "Look at the people we're attracting to this industry now."



One of those people is the former president of the American branch of Acorn Computers, Harvey Lawner. He earned his BS in computer science at City College of New York and worked for Digital Equipment Corp, Data General, and Sony before taking over at Acorn. After he had been there three years, the parent company in Great Britain decided to close its American subsidiary. Lawner had to find another position. A friend suggested that he try recruiting. He did, and he was surprised by the demands of the job.

"People think that what we do is simple, but it's quite the contrary. It's probably the most difficult thing that I've ever done," says Lawner, who is now a senior partner at Logix, a recruiting firm in Waltham, MA.

The job is demanding, Lawner continues, "because I'm dealing with people, and people are consistently inconsistent. I can show you how a workstation performs, and it'll do what it's supposed to do, but I can't control people. I can't create chemistry between two people. I can't make decisions for people. I've found this job to be a lot more strenuous and stressful than working at Acorn Computers."

Special problems with engineers

In addition to the difficulties a headhunter might run into trying to recruit any professional, engineers often present special problems. Many engineers won't change jobs simply for more money. They want to work on projects that involve the most advanced technology or offer the opportunity to develop new products. Understanding the importance of job satisfaction to engineers is one of the keys to being a successful high-tech recruiter.

David Scardifield, president of Omnisearch Inc in San Mateo, CA, is specially qualified to recruit engineers. He has a bachelor's degree in electrical engineering from Reading Technical College in Reading, England, and he has held various management positions in companies such as Honeywell and Telex Computer Products. He often dealt with headhunters when he was trying to find engineers.

"A lot of times when I was looking for field engineers I had a difficult time finding a recruiter who really understood what they were," he says. "They would send me design engineers or they would send me bench technicians. I began to see there was a market niche there for a recruiting company."

Tired of working for large corporations, Scardifield wanted to strike out on his own. "I looked at what kinds of things I might do where

the fruits or failure would be right at my own doorstep. I enjoyed the people side of technical management, and it looked to me like there was an opportunity to do headhunting in a little bit different way.

"I worked for a recruiter for a year to learn the business, then started my own company, specifically to find field engineers and engineering managers," he continues. "I did it for about a year, and I was quite successful at it. Then the companies I was doing that for began to ask me to find other kinds of people, and that's how I got into the rest of the business."

The new breed

Not all headhunters are engineers, of course, but Read, Lawner, and Scardifield exemplify the new breed. Their educational backgrounds and their firsthand knowledge of the high-tech industry have helped them immeasurably in their careers as recruiters. They speak the same language as the people they deal with, so they can tell precisely what an employer or a candidate is looking for. They can also tell if someone is stretching the truth on a resume. A good headhunter can save everyone time and money.

As the high-tech industry changed, the headhunter's job changed with it. It's no longer enough to simply find viable candidates and arrange interviews. As Read says, "Recruiters have had to become much more sophisticated and concerned with the service aspects of this business."

The service aspects may include giving candidates advice on how to write their resumes, how to present themselves to their prospective employers, and how best to leave their present jobs.

Sometimes after employees announce they're leaving, their companies will make a counteroffer. It might be a raise, a bonus, a promotion, incentives to go to school, even tenure. If the employees aren't prepared for a counteroffer, it might catch them off balance.

"I usually cover those things during the recruiting process," Scardifield says, "so the candidate has already thought it through.

"Counteroffers aren't usually effective," he adds, "because why didn't the company make that offer to the person without having to be pushed to it. Most people see that."

Other advantages for clients

Experienced recruiters can provide another advantage to both client companies and candidates—

What to do when a headhunter calls

Listen carefully. It won't cost you anything to listen. Even if the job the headhunter proposes isn't right for you, you'll gain information about the current marketplace. In addition, letting the headhunter know what you're interested in may lead to a better offer in the future.

Check on the headhunter's reputation.

- Ask your friends and colleagues about the recruitment firm and if they've ever had dealings with it.
- Call the state labor office or the Better Business Bureau where the recruitment firm is located and find out if any complaints have been made against it.
- Ask the headhunter if he or she belongs to any of the national organizations—the National Association of Corporate and Professional Recruiters (Louisville, KY), the Association of Executive Search Consultants (Greenwich, CT), or the National Association of Personnel Consultants (Arlington, VA). All three promote ethical standards for the profession and deal with complaints against their members.

Insist on confidentiality. If you give your resume to a headhunter, you have a right to know where he or she is going to send it. Recruiters have been known to mail out resumes to dozens, even hundreds of companies. This only increases the chances that news of your job hunting will get back to your boss. Tell your recruiter that you want to know in advance where your resume will be sent and insist that all efforts on your behalf be kept strictly confidential.

Arrange a personal meeting. If possible, meet with the headhunter face to face and talk about his or her experience, contacts, and plans for you. You should have a good rapport with your recruiter, just as you do with your doctor or lawyer. The recruiter's manner and appearance should also meet with your approval. Remember, this person will be representing you.

their network of contacts. If a headhunter has placed people successfully they will refer others to him or her. After being in the business for years some recruiters no longer have to make cold calls or run newspaper ads to find qualified candidates. The candidates come to them.

Dealing with an established recruiting firm has one more advantage for a candidate. Because the firm is going to be around for a long time there shouldn't be any pressure on someone to take a job he or she isn't really suited for.

The image of headhunters has also been improved by the growth of professional organizations, which set ethical standards for their members. The three major national organizations are the National Association of Corporate and Professional Recruiters, the Association of Executive Search Consultants, and, by far the largest with more than 2300 member firms, the National Association of Personnel Consultants (NAPC).

Read is a past president of the California Association of the NAPC and now serves on the national board of directors. In his home state he has been active in promoting legislation, such as the licensing of career counselors, that he believes has benefited both candidates and client companies.

"There are probably more candidates who got caught in the problems than companies," says Read. "Candidates would put their faith in a recruiter and be told information that wasn't true. It would take them down the wrong path. You can't legislate morality, but you can set up a system that clients and candidates can go to and find consistency as to what can be expected from our members."

High-tech recruiting is relatively young, but it has already passed through its childhood and its boisterous, rowdy adolescence. It has now entered its adulthood. As the industry matured most of the fly-by-night operators departed and the new breed of headhunters emerged. Lawner sums up in simple terms why they have been successful. "You have to understand what you're doing, like any other business. I think understanding your trade, understanding the service you provide, and providing that service to its completion is really what it's all about." EDN

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1990 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Feb. 15	Jan. 25	Digital ICs, Computer Systems, Interconnect Technology, Sensors
News Edition	Feb. 22	Feb. 2	CAE/Hardware, Telecom, Regional Profile: No. California
Magazine Edition	Mar. 1	Feb. 8	Computer-Aided Engineering/ASICs, Computers & Peripherals, Digital ICs/Microprocessors, Semicustom ICs
News Edition	Mar. 8	Feb. 15	Analog/ICs, Automotive Electronics, Special Supplement: RISC/Microprocessors
Magazine Edition	Mar. 15	Feb. 22	Analog ICs, Components, Engineering Software, Special Design Project #1
News Edition	Mar. 22	Mar. 2	Optoelectronics, Peripherals, Regional Profile: New York, Pennsylvania & Connecticut
Magazine Edition	Mar. 29	Mar. 8	Software Special Issue—Interface ICs, Software/Programming/Microprocessors/ASICs, April Fools Section, Special Design Project #2
News Edition	Apr. 5	Mar. 16	IC/Logic ICs, Distribution, Special Supplement: Distribution
Magazine Edition	Apr. 12	Mar. 22	Communications Special Issue—Communication ICs, Communication Systems, Microprocessors, Special Design Project #3
News Edition	Apr. 19	Mar. 30	ICs/Graphics Controllers/Microprocessors, Industrial Automation, Regional Profile: So. California
Magazine Edition	Apr. 26	Apr. 5	Computer Boards/Microprocessors, Power Sources, Sensors/Transducers, Special Design Project #4, Electro Show Issue
News Edition	May 3	Apr. 12	CAE/Board Layout, Education, Special Supplement: ASICs, Electro Show Issue
Magazine Edition	May 10	Apr. 19	Analogy Technology Special Issue—Analog ICs, Analog Instruments, Digital ICs/Microprocessors/ASICs, Special Design Project #5
News Edition	May 17	Apr. 27	ICs/Memory ICs, Test & Measurement, Regional Profile: Massachusetts & New Hampshire
Magazine Edition	May 24	May 3	Microprocessors, Computers & Peripherals, Semicustom ICs/ASICs, Components, Sensors & Transducers
Magazine Edition	June 7	May 17	Software, Design Tools, Microprocessor I/O Chips, μP Support Chip Directory
News Edition	June 14	May 24	Peripherals/Input Devices, Software, Special Supplement: EDA
Magazine Edition	June 21	May 31	Computer-Aided Engineering, Computers & Peripherals, Power Semiconductors, Semicustom ICs/ASICs
News Edition	June 28	June 8	ICs/RISC/Microprocessors, Image Processing, Regional Profile: Oregon & Washington
Magazine Edition	July 5	June 14	Product Showcase—Volume I: Hardware & Interconnect, Power Sources, ICs & Semiconductors, Software
News Edition	July 12	June 21	Analog/Communication ICs, ASICs, Special Supplement: Automotive Electronics, Regional Profile: Washington, D.C.
Magazine Edition	July 19	June 28	Product Showcase—Volume II: CAE/ASICs, Computers & Peripherals, Components, Test & Measurement
Magazine Edition	Aug. 2	July 12	Digital ICs/Microprocessors, Computer-Aided Engineering, Computers & Peripherals, Test & Measurement, Technical Article Database
News Edition	Aug. 9	July 20	CAE/Software, Aerospace, Special Supplement: Defense
Magazine Edition	Aug. 20	July 30	Military Special Issue, Vision/Image Systems, ICs & Semiconductors, Memory Technology, Software
News Edition	Aug. 23	Aug. 3	Electromechanical, Opportunities in Non-EOEM, Regional Profile: New Mexico, Arizona

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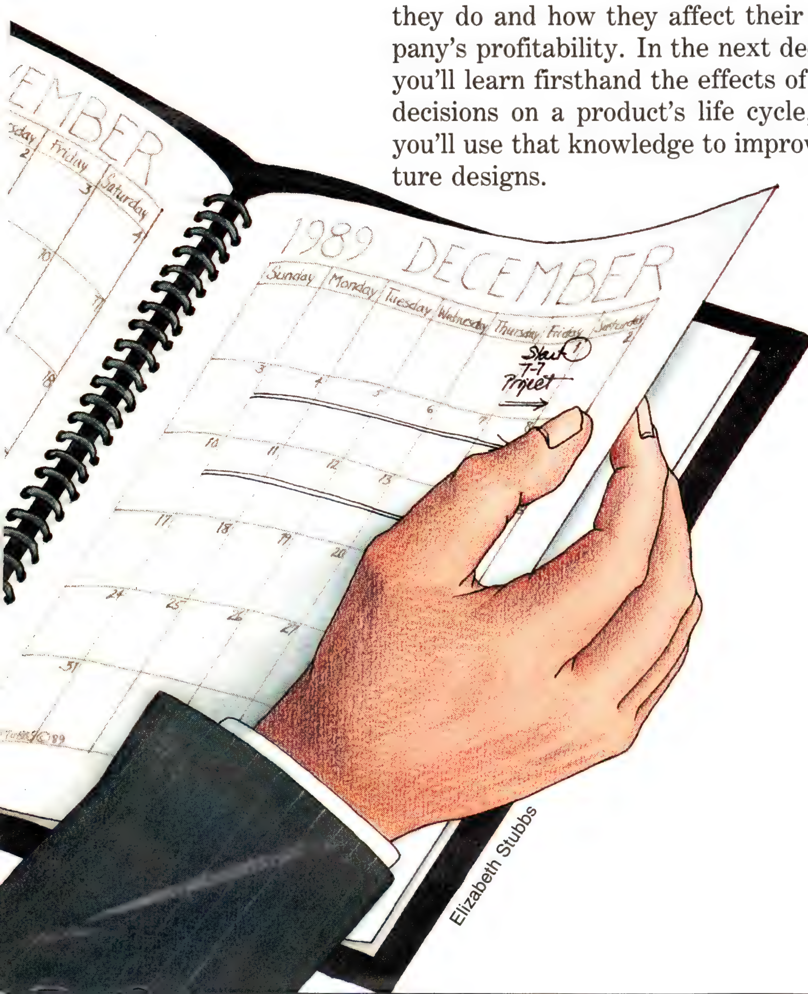
EDITED BY JAY FRASER

Engineering in the 1990s

EDN's editors predict how your job will change in the coming decade.

In the 1990s your job and your responsibilities as an engineer or engineering manager will expand dramatically. The days will soon be gone when you simply hand a design to the people in manufacturing and let them take it from there. In the years ahead you'll be much more involved in financial and manufacturing decisions. You'll follow your designs through the entire manufacturing process and into field service. You'll even be dealing with the customer-relations department and sometimes with the customers themselves.

Your new cradle-to-grave responsibility for your designs will help you in your work. Today few engineers know, or are told, the overall implications of what they do and how they affect their company's profitability. In the next decade, you'll learn firsthand the effects of your decisions on a product's life cycle, and you'll use that knowledge to improve future designs.



Because it will be practically impossible for them to undercut their Asian rivals on price, US companies will place new emphasis on service. You'll be meeting customers to explain the subtleties of your designs, how you ensure quality control, and what you do to produce a reliable product. This change in your responsibilities means you'll have to polish your interpersonal skills.

One vision of the decade ahead conjures up a nightmare in which engineers are chained to their workstations and confined to very small areas of specialization. We believe this scenario is ridiculous. You'll probably have to become familiar with a larger number of computer systems and software packages, but the storage, modeling, analysis, and communications capabilities of your workstation will let you take on larger and larger projects at higher and higher levels of abstraction. Instead of narrowing, your horizons will broaden.

Workstations will become much more sophisticated in the 1990s. For example, instead of telling you only whether a design will work or not, your new CAE and electronic design automation (EDA) tools will give you much more detailed information on how to change your designs to better meet your projects' goals. You'll be freed from repetitive, time-consuming tasks and have more time for creative thinking and experimentation. CAE and EDA are going to reverse Thomas Edison's rule: Engineering will become 90% inspiration and 10% perspiration.

However, no matter how sophisticated computers become, they will never be able to replace that old standby—the prototype. It's just not worthwhile to develop computer programs that can simulate the operation of complete and complex systems. You'll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REAL-TIME

still be getting your hands on real hardware.

Engineering will continue to require a mixture of hardware and software skills. Although software seems to dominate many of today's projects and products, in the next decade there will be a definite movement back to hardware design. In many designs it's already easier to change the hardware than the software.

Hardware design will change, too. Manufacturing processes will incorporate new techniques and methods, and you'll be called upon to improve the reliability of your designs. To do that you'll have to become even more involved with reliability engineering and failure analysis.

Soon computer-aided software-engineering tools will progress beyond their current disjointed state, and software engineers will become more like systems designers. You'll be working on "abstract" problems the way IC engineers now work with block diagrams and equations instead of the actual transistors and physical layouts on silicon chips. You'll be defining problems in conceptual terms rather than plotting instruction-by-instruction design strategies. The use of object-oriented programs and object-oriented languages such as C++ will change the way you think about programs and how you solve software problems.

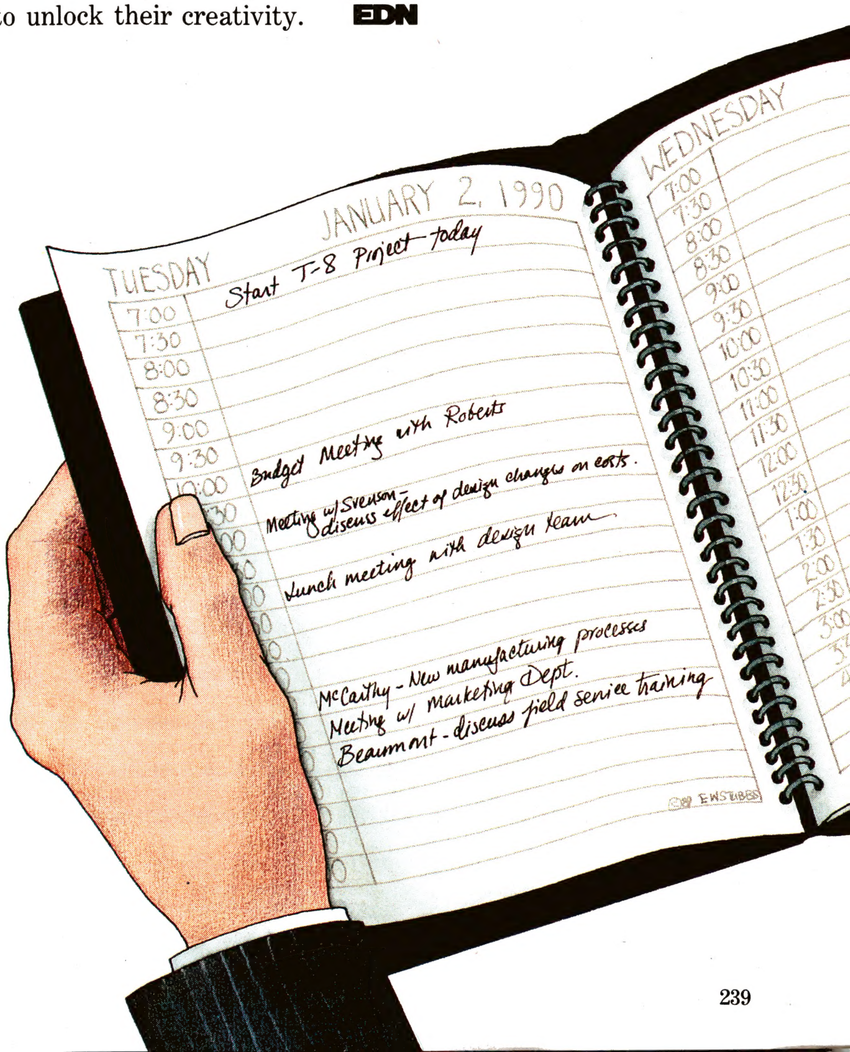
Computer-aided software engineering will have an impact on the software engineer's job similar to the impact CAE has already had on the hardware engineer's. Software engineers will function in the same way systems design integrators do now. They'll start with definitions of "software requirements" and broad goals.

If you're an analog engineer, your job will also change. You'll find yourself working more as a device engineer does, building and analyzing ultrafast ICs. The use of simulation will grow, but you'll continue to test your designs through experimentation. As far as we can see, device models will never be accurate enough to do away with it.

Unfortunately, the ranks of analog engineers will shrink; they are already retiring faster than they are being replaced. Digital engineers will have to try to solve some analog problems—a situation that seldom delights digital engineers.

In the 1990s, your job as an engineer or engineering manager will be much broader and will require a broader vision. You'll have to be able to see beyond components and circuits, beyond systems and networks. You'll have to be able to see the entire life cycle of what you design; how it will be manufactured, marketed, and serviced; and how it will affect people's lives.

Engineers who can't develop this vision will be relegated to support functions. They'll use design tools, but they'll only implement other people's designs. The engineers who will be successful in the next decade will be those who use their engineering training as a key to unlock their creativity. EDN



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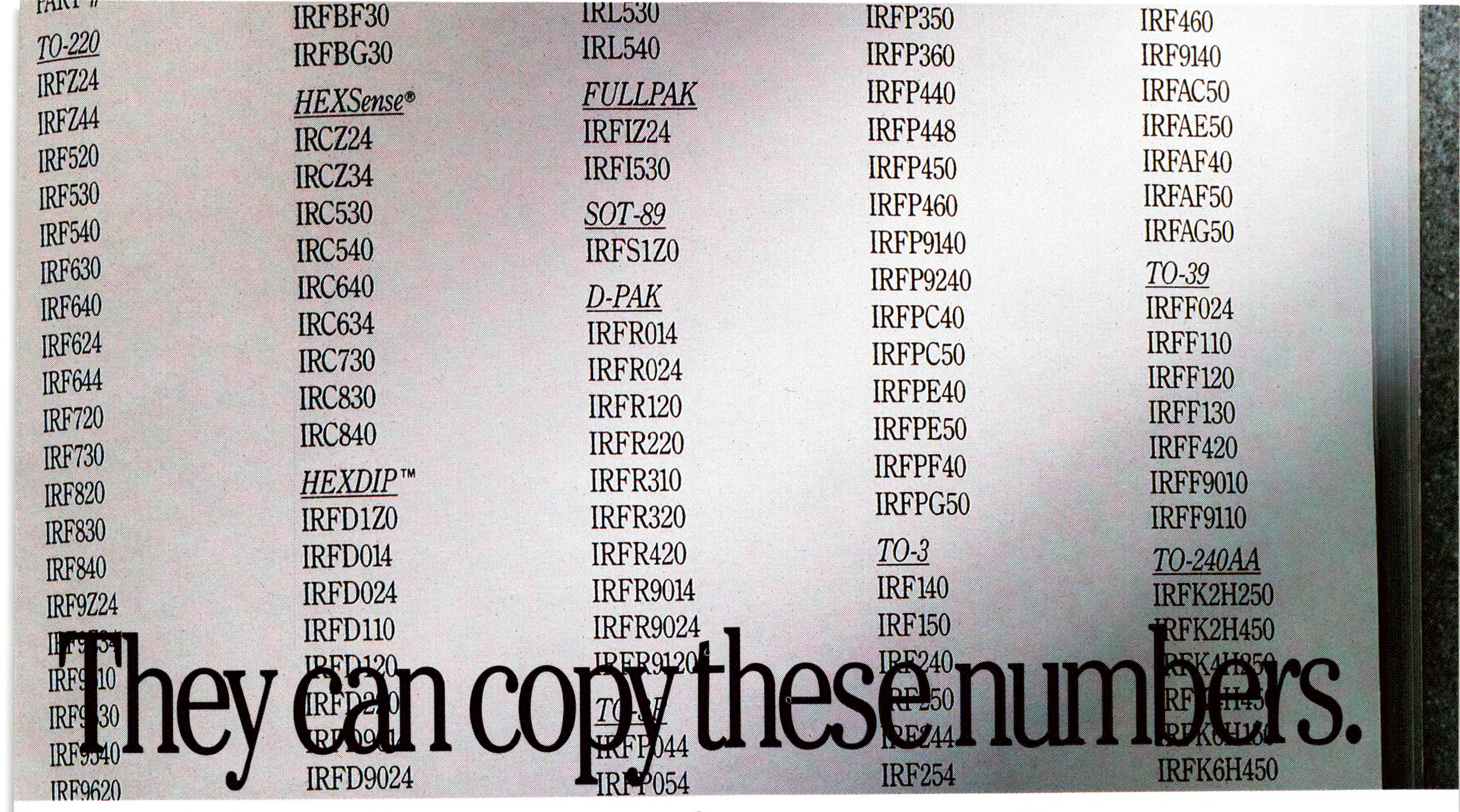

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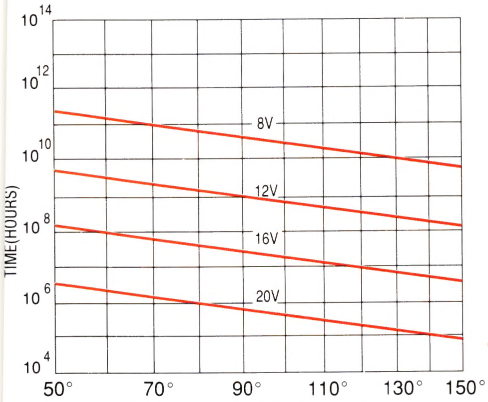

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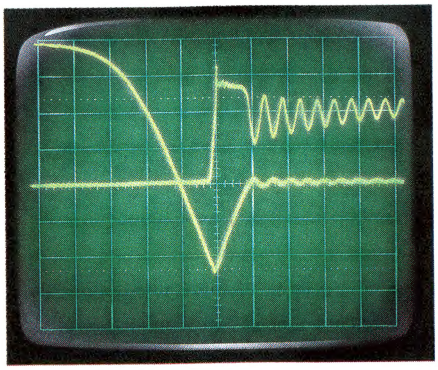

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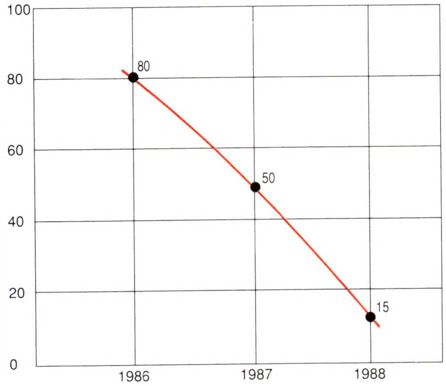

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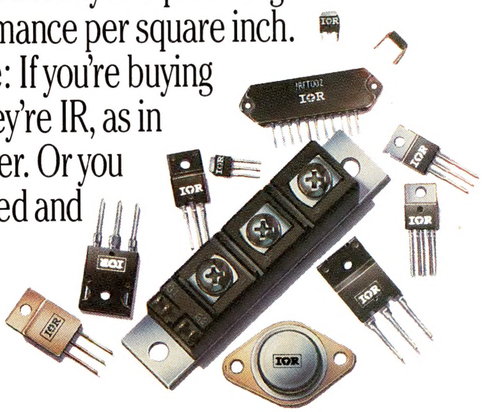

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PROGRAMMING TECHNOLOGY THAT SUPPORTS ADVANCED DESIGNS— TODAY AND TOMORROW. The UniSite™'s universal programming technology is the fastest and easiest way to keep up with new devices and packages. Its software-configured pin driver system provides a single site for programming any DIP device up to 48 pins, including PLDs, PROMs, IFLs, FPLAs, EPROMs, EEPROMs and microcontrollers.

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